Design of Test Modules for the Analysis of MCM Interconnects
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Abstract
A thin-film Multichip Module (MCM-D) switching unit, specifically designed for performance analysis of interconnection substrates, is described. A test approach is presented for the characterisation of a given device technology as a function of geometrical, physical and electrical quantities - in this particular case, a MCM-D technology and a 0.7μm CMOS technology.

Introduction
Thin film MCMs [1] provide a high packaging density. The short interconnection lengths on MCM-D enable high speed digital operations. The analysis of the limits of the high speed performance of such a technology is a challenging task. Individual nets on the substrate are difficult to contact during operation of the module and measuring nets using hf-probes may very well influence the operating conditions of the module. A possible solution to this problem, especially suited for digital applications, is presented here. This solution provides a way to analyse the performance of a module as a function of geometrical, physical and electrical quantities as well as circuit and system parameters. This solution can bring useful information to MCM manufacturers on the system performance and operation limits of their products, as it can be used for technology validation.

Test methodology and MCM design
The system working frequency is determined by signal integrity, propagation delays, power dissipation, crosstalk and switching noise, which are influenced by geometrical, physical and electrical quantities such as line width and dielectric thickness, losses, driver size [2]. To analyse this influence, a test approach was developed based on the design of a test module consisting of 4 identical bare 0.7μm CMOS ASICs (100 I/O's, 64mm²) switching data at 200 Mbs on a five layer MCM-D (1"x1", 2 signal layers). The four chips are programmable and provide a total of 64 high frequency channels. The same pattern is transmitted on these channels while increasing the clock frequency. It is thus possible to link the frequency point of the first error occurrence to the channel length, relating in this way working frequency and line length. Other quantities are analysed in this way: crosstalk, switching noise, driver type, line load and so on. Figure 1 shows the layout of the active test module used for the implementation of the test methodology. The substrate contains 400 bonding pads, 44 I/O pads, 8000 thermal vias, 2071 electrical vias, 96 nets and 3.7m of total routed length. The packaging efficiency is 40% (wire-bond limited). Trace width and via size are 30μm; dielectric layers are up to 10μm thick [3].

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Conclusion
A means for system performance evaluation of an interconnection technology for high speed applications has been presented. The use of a common benchmark vehicle allows for an easy validation of different technologies. A MCM-D switching unit has been developed in IMEC for the implementation of the test methodology.

References