TRJM: A High Speed Programmable ATM-SDH Mapper

J. Crespo, F. Calvo, J. I. Solana, R. Caravantes, J. L. Conesa

TELEFONICA I+D

Abstract

This poster presents the design of the TRJM integrated circuit. This ASIC has been developed to implement the ATM transmission convergence sublayer interfaces for different SONET rates and its SDH equivalents. The chip has been manufactured using a standard cell 0.6 microns 3-layer metal CMOS technology. It contains 350,000 transistors split in 42 K gates and 18 Kbit from dual port RAM.

The basic function of this chip is to insert and extract ATM cells from a SDH or SONET frames. The chip can be configured to work with multiple line interfaces allowing bidirectional SDH-ATM flow and handling different synchronous frame structures in transmission and reception. It can manage directly data rates up to 155 Mbit/s synchronous frame structures. The 622.08 Mbit/s data rate need to be parallelized to eighth lines at 80 MHz. It also manages SONET 51.84 Mbps data rate.

To ease the design process and obtain a good flexibility, it was split into different blocks depending the kind of structured handled and the flow direction (transmission and reception).

Decoupling memories were necessary to put between ATM process and SDH one. The figure shows the block diagram of the chip.

For such a complex design like this, an initially description at behavioural level using Verilog HDL language was developed making 10,000 line code. After that, an RTL Verilog description was done for each block to validate it.

Synopsys synthesis tool was used to map into a gates from the RTL description. Different description approaches were necessary to make in conflicting blocks due to the high speed requirements (80 MHz internally frequency clock at the most demanding mode).

Due to complexity to assembly and disassembly SDH / SONET frames and the capability of the chip to handle different data rates, millions of vectors was necessary to check the functionality of the circuit. To stimulate the circuit, high level Verilog description was developed for every mode that can be programmed the chip. Previously, each block of the circuit was checked alone in the same manner.

Full scan strategy was chosen as the best approach to the test requirements for this design. To connect the scan flip-flops, an automatic chain generator was implemented to minimize area overhead due to chain routing. Finally, the vectors was generated applying an ATPG tool.