Quiescent Current Estimation for Current Testing

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Abstract

Logic voltage testing has some limitations dealing with defects that turn digital into analog values. For these parametric faults, current testing is being considered as a promising complementary technique. In this work, a methodology to characterize the quiescent circuit consumption in a new way that simplifies the electrical simulation of a complex VLSI circuit is proposed. Further it is exemplified on the C17 ISCAS circuit, concluding that the proposed method has been successful in the example and can be easily programmed to estimate \( I_{ddq} \) for large circuits without the well-known electrical simulation time penalty.

Keywords: Current testing, quiescent current, current sensing, gate oxide shorts, floating gate opens, bridging defects.

1 Introduction

Well-known fault models as stuck-at, stuck-open and stuck-on, used in logic voltage testing, have been proved insufficient to model some defects, especially in CMOS circuits. Shorts and breaks in different conductive levels have been reported as more realistic defect mechanisms in VLSI circuits [15] causing some parametric errors that cannot be detected by voltage testing. For these failures, quiescent current testing is being considered as a good complementary test technique in CMOS technology [5], [7], [8], [16].

The design of the current sensor [12] requires the estimation of the range of \( I_{ddq} \) currents in the presence of current sensitive defects. This information will be used to adjust the level of comparison of the current sensor.

To estimate the quiescent current consumed by a defective circuit the following methods have been used with different degrees of success:

A) Electrical or mixed level simulators using the electrical models of each defect [4], [11].

Advantages: High precision of the estimated analoge currents and voltages. Disadvantages: The size of the defective circuits modellable is relatively small. The method is time consuming. For each defect characterization a simulation run is required.

B) Switch level simulators with switch models for the defects [6], [17].

Advantages: The size of the modellable module increases in front of methods of type A). Disadvantages: The precision of the estimates due to crude switch level defect models could become insufficient to predict the analoge ranges of the quiescent currents and voltages.

C) Experimental quiescent current measurements on defective circuits [16], [19].

Advantages: Gives the best estimates for the class of circuits measured. The process conditions need to be maintained and the defects present in the samples measured should be representative. Disadvantages: High cost of experimentation. Difficulty to extrapolate the values measured when the process changes or on other circuits \( I_{ddq} \) levels have to be estimated.

This paper proposes a new methodology to characterize the quiescent consumption of CMOS circuits in a way that simplifies the electrical simulations of a complex VLSI circuit. Section 2 presents the characterization methodology proposed based on presimulation of the defects at electrical level only for the subcircuit that presents non-digital behaviour. This procedure is exemplified over C17 ISCAS circuit in section 3. Finally, in section 4, some conclusions are given.

2 Defective and analog Penetration Subdomain Characterization

This section shows a proposal for \( I_{ddq} \) characterization based on presimulation of the defects at electrical level of a subset of a complex circuit. This subset will be called the Analog Domain of the defect.
2.1 Analog defective subdomain

In this section we characterize the Analog Defective subdomain for faulty circuits in the presence of a large class of realistic defects. The electrical models used for each defect can be found in [2].

The defective subdomain of the defect will be characterized and precomputed. It will be called the analog macromodel for the defective subdomain. The data information needed to do the forecast will be catalogued and applied to different target circuits.

BRIDGES. A bridging defect is produced by a short between two nodes \( i, j \) of the circuit. The characterization will be done by its resistance value named \( R_b \). Depending on its value, the circuit may work logically correct or not and may consume an abnormally elevated quiescent current [10]. This quiescent consumption will denote the presence of the bridge.

All possible shorted node combinations can be reduced to three classes of bridges:

- **Class A**: Bridges involving internal and output nodes of a single module. The defective module constitutes the analog defective subdomain.

- **Class B**: Bridges involving one input node and one internal or output node of the same module. The analog defective subdomain has two modules: the module (gate) with the internal or output bridged node and the module driving the bridged input.

- **Class C**: Bridges between one output or internal node of module \( i \) and one output or internal node of another module \( j \) not connected to module \( i \). The analog defective subdomain is composed of the module \( i \) and the module \( j \).

In conclusion, for bridges, the size of the analog defective subdomain is one module (class A) or two modules (class B and C).

GATE OXIDE SHORTS. For this defect a conductive path is created from the gate of the defective transistor to its channel [3], [14]. The GOS will be characterized by giving its location into the channel and its resistance.

For the GOS defect the isolating property at DC of module to module is lost just in the transistor with GOS. Basically, there can be two contributions to the \( I_{ddq} \) current. One, called the main current, is the current flowing through the oxide short. The other contribution, called secondary current, appears because some of the inputs of the gate with the GOS defect are at an intermediate voltage between the (L) and (H) logic voltages.
The analog defective subdomain includes de module with the GOS transistor and the driving module generating the input connected to the transistor with GOS.

FLOATING GATES. The Floating Gate defect is due to an open in the transistor gate poly lead. The behaviour of the Floating Gate defect depends strongly on the coupling capacitances of the transistor device and on the surrounding circuitry.[2],[4],[9].

The parameters to characterize the defect are: the capacitance poly-bulk $C_{pb}$ and the capacitance metal-poly $C_{mp}$. Depending on these values it can be estimated the abnormal current consumption and the output voltage of the faulty circuit. To take into account opens that affect both, PMOS and NMOS transistors, the double transistor with floating gates has been considered.

Because the Floating Gate defect isolates at DC the driving module to the module with the defect, it will not propagate to the driving module. And, due to the MOS transistor gate isolation, it is not propagated to the load. Then, the Analog Defective subdomain for a circuit with one or more FG’s at the same module is limited to the defective module.

For the Defective Subdomain Characterization we have obtained different tables showing these analog macromodels for different driving-loading configurations and the three analyzed defect types. The macromodels have been obtained by SPICE simulations of the ADS with ES2 1.5µm parameters. Section 3 shows the application of this macromodels in a circuit characterization example.

2.2 Analog Penetration Subdomain

We have defined the Analog Penetration Subdomain [13] as the set of fault free stages that exhibit an abnormal value of I_{ddq} because of non-digital input values. The Analog Penetration Subdomain is equivalent to $r$ sub-trees that start from the node (fan-out equal to $r$) that takes the analog voltage $V_N$. The Analog Penetration Subdomain limit depth ($d$) quantify the penetration level of the analog fault effects in the logic network.

This penetration depth has been found to be small in the analyzed circuits. This fact is due to the nature of the transfer characteristics of the full complementary CMOS gates. For this class of gate realizations, an intermediate analog voltage is quickly amplified until enters the digital specified ranges.

$$\begin{array}{|c|c|}
\hline
V_N & \text{limit depth } d \\
\hline
> V_{DD} - V_{TP} & 0 \\
1.50 & 1 \\
1.70 & 2 \\
1.80 & 2 \\
1.85 & 3 \\
1.87 & 4 \\
1.89 & 3 \\
2.00 & 2 \\
2.10 & 2 \\
2.20 & 1 \\
< V_{TN} & 0 \\
\hline
\end{array}$$

Table 1: Values of the limit depth for different input voltages in CMOS technology

The type of stages forming the APS influences the value of $d$. For a tree of inverters the limit depth $d$ can be calculated as follows:

If the Static Transference Characteristic of the inverters is given by function $STC$ in such a way that, $V_o = STC(V_i)$, where $V_o$ and $V_i$ are the input and output voltages of the inverter stage, the limit depth $d$ is given by the lower integer that verifies one of the two next conditions:

$STC^d(V_N) < V_{TN}$,

$STC^d(V_N) > (V_{DD} - V_{TP})$,

where $STC^d$ means the $d$-th self-concatenation of function $STC$, and $V_{TN}$ and $V_{TP}$, the threshold voltages of the MOS transistors.

The additional current due to the analog fault ($V_N$), $I_{ddq(APS)}$ is composed by the aggregation of $I_{ddq}$ components, with one component for each stage of the Analog Penetration Subdomain.

If we call $d_{max}$ the maximum limit depth of the Analog Penetration Subdomain and $w_j$ the tree width for depth level $j$ we can write:

$$I_{ddq(APS)} = \sum_{j=d_{max}}^{\infty} \left( \sum_{i=1}^{\infty} I_{ddq_{i,j}} \right)$$

where $I_{ddq_{i,j}}$ represents the $I_{ddq}$ current of the stage $i,j$ of the APS, $w_j$ takes the value $r$ for $j=1$. When $d_{max}=1$ the Analog Penetration Subdomain is limited to $r$ components corresponding to the fan-out factor. Table 1 shows the penetration factor $d_{max}$ for a chain of inverters and different analog inputs. Although it is theoretically possible to get unlimited penetration levels, it can be concluded from the Table 1 that, for analog voltages slightly separated from the voltage that gives the maximum current, $d_{max}$ takes very low values.
For the inverter circuit it is well known the relation between \( v_{\text{input}} \) and the Vdd-Gnd current. The equations can be obtained from the static MOS model of Sah. The maximum \( I_{\text{ddq}} \) value, \( \text{MAX}(I_{\text{ddq}}) \) corresponds to \( v_{\text{input}} = V_D / 2 \) for an equilibrated technology. In this case, \( v_{\text{out}} = V_D / 2 \) and the value of \( d_{\text{max}} \) may take a large value, infinite theoretically. Realistic values of \( d_{\text{max}} \) are lower than 1 for technologies with characteristic deviations in the order of 1% as it has been shown in Table 1.

Furthermore, in multiple input gates, some digital inputs will force the output of a gate with analog inputs to fall directly into the digital specified ranges. If an input variable forces one of the following conditions at the output:

\[
\begin{align*}
(1) \quad & V_{\text{out}} < V_{\text{Tn}}, \\
(2) \quad & V_{\text{out}} > (V_D - V_{\text{PP}}),
\end{align*}
\]

then \( I_{\text{ddq}} \) is null, independently on the value (digital or analog) of the other inputs.

3 Circuit characterization methodology: C17 ISCAS circuit example

This example shows the voltage and \( I_{\text{ddq}} \) characterization procedure for the C17 ISCAS circuit with the three studied defect types. Figure 2 shows the general scheme for the methodology and the work accomplished in the example. Three different phases can be distinguished: Module Library Characterization, Fault List and Test Vector Set Generation, Voltage and \( I_{\text{ddq}} \) Computation.

The results of this computation are obtained as total defective \( I_{\text{ddq}} \) currents and output voltages. Figure 3 resumes in a Bar-Diagram the results for the example with a simplified fault list of 12 representative cases.

As can be seen in this Result Bar-Diagram, \( I_{\text{ddq}} \) currents for Bridge and GOS defects are very dependent on Resistor parameter value. Nevertheless in the worst case (79\( \mu \)A in case 6) the current is big enough to be discriminated by a sensor. Floating gates, in general, show smaller \( I_{\text{ddq}} \) values than its companion defects, with the two double floating cases reflecting larger currents than single opens.

Finally, it is interesting to look at the difference between the Analog Propagation Subdomain and the Analog Defective Subdomain. These two domains are represented in Figure 3 by the black and the dashed shadow patterns respectively.

As first conclusion the currents due to the defective subdomain can be smaller than those due to the penetration effect. Case 7 and case 12 are good examples of better penetration currents. The penetration effect disappears, in defects caused by shorts (Bridges and GOS) when the resistance parameter is high. In this case defective subdomain currents are small but discriminable. For Floating Gates, the influence over the two transistor gates is sufficient to spread the defect and generate currents in the penetration subdomain with higher values than in the defective subdomain (see cases 11 and 12).

4 Conclusions

A new methodology for \( I_{\text{ddq}} \) estimation in complementary CMOS integrated circuits has been proposed. The analog macromodels for the defective subcircuits have been presented for different defective parameters and later used in the estimation of \( I_{\text{ddq}} \) for a given circuit with a defect list.

The following facts have been found:

- The Analog Macromodels are obtained simply by evaluating their quiescent behaviour with analog inputs.
- The Defective Subdomain is composed of one or two modules for the studied defects.
- The Penetration Subdomain has been found to be composed by few stages. Rapidly the digital voltages are recuperated.
- The size of the ANALOG DOMAIN of the defective circuit depends on the defect and its location, but not on the global size of the circuit under test.

The methodology proposed has been successful for a small circuit and can be easily programmed to estimate \( I_{\text{ddq}} \) for large circuits without simulation time penalty.

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Figure 2: Methodology General schematic

Figure 3: Results bar diagram for C17 ISCAS example.
References


