Can Supply Current Monitoring be Applied to the Testing of Analogue as well as Digital Portions of Mixed ASICs?

VLSI Design & Test Group, Dept. of Electronic Engineering,  
University of Hull, Hull HU6 7RX, U.K.

Abstract

This paper is concerned with investigations into the suitability of supply current monitoring as a technique for the testing of analogue circuit modules. Iddq monitoring is already recognised in the digital field. The possibility of a unified testing approach for mixed ASICs is raised. The potential effectiveness of the method is investigated. Simulation results are reported to illustrate typical supply current levels for nominal and defective circuits. Analogue fault detection by this technique is compared with detection by observation of the circuit's output.

Introduction

Mixed analogue and digital ASICs are now widely available and offer considerable advantages in terms of cost, flexibility and reliability. There are however considerable difficulties in determining strategies for testing and design for testability specifically for such mixed devices. There are well established Design for Testability (DFT) and Automatic Test Pattern Generation (ATPG) techniques for the digital portions of chips. This is not so for analogue parts of the circuitry.  
The function/behaviour of any analogue block is very 'context specific' and hence so are its test requirements. It has been stated that "the general analog test problem is intractable" [1], but a number of DFT techniques have been proposed to assist macro specific testing, eg. signal multiplexing [3], use of MOS switches to isolate filter stages [1], analogue 'test tables' [2], analogue 'scan-path' [4], etc.  
These approaches to mixed test require a careful partitioning of digital from analogue sections of a chip. This satisfies controllability and observability requirements to permit the separate testing of each section.  
Other work has suggested adopting a unified approach to mixed testing. In [5] carefully characterised test stimuli are injected at the inputs of a mixed circuit to excite a transient response from the circuit capable of propagation in both analogue and digital parts. Diagnosis is then made by analysis of this transient response.  
Since two stage testing has a cost penalty, the potential benefits of developing techniques which permit the testing of both categories of circuit with the same equipment are significant.  
A great deal of interest has been shown recently in supply current monitoring for testing of CMOS logic circuits [7,8]. The current passing through the VDD or GND terminals is monitored during application of the input stimulus. In the quiescent state circuits draw a very low current (nanoamp levels); for certain input states this current is raised to abnormal levels by the presence of defects. The technique has a number of important advantages. It can indicate a defect directly, with no requirement to propagate the effects to an output pin. Also it is capable of detecting defects which are missed by the traditional testing method for digital CMOS ICs, which uses the stuck at fault model. Fritzmeier, Soden et al. reported increased coverage with significantly reduced sets of test vectors [11].  
Initially there were a number of limitations with the technique. However, these were mainly the consequence of off chip sensing, and have been largely circumvented by the development of built in current (BIC) sensing using on chip sensors. Prototype BIC sensors have been built by other workers and shown very effective [8]. The method is seen as both sensitive and comprehensive, particularly useful for the testing of high quality, high reliability ICs.  
The advantages offered by current monitoring in the digital field have prompted these investigations into whether this or a similar technique can be applied to the process of analogue testing. Practical experience has demonstrated that using current monitoring as a preliminary screening test can eliminate a large number of faulty chips. In [9], when applied to certain prototype circuits and even though screening only for extreme
current changes, 100% correlation with functionality was found.

The intention of this work is to maximize the usefulness (coverage) of this stage, to investigate whether a rather crude technique can be rendered more sensitive. The more faulty chips which can be eliminated quickly, the more time there is available for extensive testing of those remaining. As with the testing of digital circuits, the proposed methodology envisages separate sensing for each module on a chip. It is similarly anticipated that on-chip sensing of analogue blocks may prove more discriminating than gross off-chip sensing. This raises questions of partitioning methodology and sensor design of course. The philosophy behind this work was discussed in [6].

Approach

Some simple analogue circuit elements (opamps) were investigated, by simulation, to determine if supply current levels would vary in the presence of defects, and if so, by how much. All simulations were performed using the SPICE circuit simulator. Initial investigations concentrated on the introduction of 'hard' faults into the circuits under test. A variety of opamps were simulated, ranging from a simple 9 MOSFET example to a more complex 20 MOSFET example.

![Fig. 1: The Fault Model](image)

The fault model [fig.1] is described in [10] and is based on open circuits in the diffusion and metallization layers and shorts between adjacent diffusions and metallizations (ie. open drain and open source contacts, gate to drain shorts and gate to source shorts). Statistically these are the more common defects.

Initially simple DC test inputs were used, exercising the opamps in their linear region. In only a small proportion of cases (approx. 16%) did the presence of defects result in an 'Iddq like' order of magnitude increase in supply current levels. Typical changes for the larger opamp were in terms of tens of microamps (from a nominal level of approx. 90 microamps). Unlike Iddq testing, the presence of a defect was as likely to cause a reduction in supply current rather than an increase.

Nevertheless, the changes in current were seen as significant. A variety of DC input combinations were tried in an attempt to elicit greater responses in terms of current change in the presence of defects. Switching between the extremes of the supply rails was found to be the most revealing (order of magnitude increase in supply current in 39% of cases). Typical results are quoted below (fig. 2). A breakdown is also given of the percentage of short circuit defects and open circuit defects detected. Results are given assuming changes of at least 25%, at least 50%, and >100% from nominal supply current levels as being necessary for discrimination.

![Fig. 2: Opamp: typical detection rates](image)

If such changes can be regarded as significant, allowing for the effects of tolerance, a high proportion of 'hard' defects can be detected by monitoring supply current and using simple DC testing.

In the digital field prototype BIC sensors have been constructed with a resolution of 2 microamp [8]. Although it is not yet apparent what might be the best form and position for current sensors for analogue blocks, simulation results were analysed assuming sensor resolution approaching this sensitivity.

The analysis was made in terms of the direction of supply current shift as inputs were changed. By noting simple relative changes rather than absolute values, it was hoped to obviate the effect of global parameter variations. Detectable current increases were classed as '1', decreases as '-1' and no apparent change as '0'. In this way 'fault signatures' were built up as a sequence of changing digits compared with a nominal condition of all zeroes. It was found that good coverage could be obtained even with this simple technique. Typical results
showing percentage detection of defects with varying assumed sensitivities of sensor were reported in [12].

In addition, a number of simulations were performed whilst varying the voltage bias on the first stage of the opamp under test. Using the same detection criteria as above, it was found that increasing the bias voltage significantly improved the detection rate [fig. 3].

The effect on coverage of increasing Vdd levels on the circuits being simulated was also investigated. Supply current was found to rise with increasing Vdd level. Percentage changes, being relative figures, remained similar at all levels of supply voltage, but the absolute values of changes were increased.

\[ V_{dd} \]

Fig. 3: Effect of varying primary stage bias

When the figures were analysed in terms of assumed sensor resolution, there was found to be a definite improvement in detection rate with increased supply voltage. This, plus the improvement with increased bias, may have implications for improving testability in this context.

Application to soft faults?

Investigations were also made into the capacity of supply current monitoring to detect the more subtle, soft or parametric faults. As an example the detectability of leaky p-n junctions was explored. The defect was modelled as a resistor in parallel with the MOSFET concerned, the 'leakier' the junction, the smaller the value of the resistance. Simulations were run using resistances of 100kohm, 1 Mohm and 10Mohm.

Detection criteria were as above. As might be expected, it was found that the 'leakier' the junction the better the chances of detection by current monitoring. The results indicated increased detection in closed loop mode [fig. 4].

Simulations on other opamps confirmed these findings. With the smaller opamps, detections was better with switching between the extremes of the supply rails, but with larger opamps there was only a slight difference in detection rates between this type of stimulation and small range switching.

Leaky p-n junctions

Fig. 4: Detection rates for leaky p-n junctions

Use of AC inputs

An extensive series of simulations was run on the example opamp circuits, in nominal and faulty states, using AC inputs, initially a single 1kHz sine wave input. Only small changes in supply current (nanoamp levels) were obtained in the presence of defects, with little improvement in detection using higher frequency inputs.

Only by greatly increasing the amplitude of the input sine wave from its original 200mv was it possible to improve coverage. Even then, coverage varied considerably between opamps. It was concluded that there was little to be gained from using AC inputs, the results from simulations using DC inputs being better and more consistent across the range of examples used.

Application to other analogue cells

Investigations thus far had concentrated on opamps. It was obviously necessary to examine other categories of analogue circuit module to determine the extent of applicability of current monitoring techniques.

Example cells from a commercial analogue cell library were investigated. Simple DC inputs were used during simulation to permit monitoring of supply current during normal functioning (rather than use of extreme inputs as with opamps). Typical detection rates are quoted for a comparator cell, voltage reference, and output buffer together with opamp figures for
comparison. To give some indication of size/complexity, these cells contained from 9 to 15 MOSFETs.

When considering changes >100% of nominal, the detection rates for bias generators and output buffers were slightly better than those for opamps, those for the comparator not as good [fig. 5]. In every case, detection rates for short circuit defects were better than for open circuit defects. Nominal currents for these cells varied from <10 microamps for the bias generators to 380 microamps for the buffer. For the bias generator however the current changes were in terms of thousands of microamps, for the buffer and comparator, hundreds of microamps.

Increasing the specified supply voltage levels during simulations produced results for each of these cells similar to those reported above with opamps.

On the whole it was found that percentage changes in supply current were much greater than percentage changes in output voltage in the presence of defects, suggesting that monitoring of supply current is more revealing of faults than simply monitoring the output voltage. The exception was in the case of the comparator cell under circumstances in which the nominal output state was low, when output voltage changes were more revealing. In the nominal high state it followed the general trend.

These findings were confirmed by a brief series of simulations with a simple Digital to Analogue Convertor (DAC). It is particularly significant that in 25% of cases the presence of a defect was revealed by supply current changes, but not indicated by any alteration in output voltage. Within the DAC, a random selection of MOSFETs in turn had leaky p-n junctions simulated. In 4 out of 5 examples these defects were detected by supply current changes, but in only 1 example was there a change in output voltage.

This suggests that current sensing promises a better coverage than monitoring voltage changes at outputs. Improved coverage by voltage monitoring requires access to a number of internal nodes, with consequent penalties. Adding pins may greatly increase package cost [9]. Multiplexers may result in unacceptable performance degradation with high precision circuits.

On the other hand, the current sensing approach has its own penalties. BIC sensors must be introduced into the circuit to be tested. It may be that a sensor is required for each module within a circuit. There is also the question of how such additional circuitry may itself affect yield.

**Conclusion**

These initial findings demonstrate that current sensing may be useful in analogue as well as digital testing; thus, in answer to the question posed by the title, a guarded 'yes'. This raises the possibility of simultaneous test of analogue and digital modules on the same chip and/or testing with same tester. As with Iddq monitoring, analogue current readings would be taken after digital switching transients had died, reducing the problem of digital tester noise affecting analogue measurements.

Further work is certainly justified. It is intended to investigate how supply current changes when defects are introduced into larger macros composed of several cells, ie. to determine how partitioning should be approached, and where sensors need to be placed. Other than