Keynote Speaker I

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Title: Design of Behaviors that Bridge the Growing Function to Physics Divide

Abstract:
When computational solutions were introduced to the design of physical system behavior, for example, in the form of digital control, embedded dedicated computational resources were outfitted with isolated computations. Over the following half century, the functionality that is accounted for in computation has grown by leaps and bounds, driven by the increasing availability of computing power and the unparalleled behavioral flexibility of software. Model-Based Design has become key in overcoming the challenges of programming software systems. As a consequence of the growing complexity of computational functionality more sophisticated language features are increasingly necessary at the model level. Original single-rate feedback control that operated on a dedicated resource has given way to support for multiple rates that may be partitioned into multiple tasks and that are executed on multiple resources. Moreover, models must provide support for task execution beyond multiple rates to allow aperiodic behavior of different initiators. In addition to this evolving complexity of function, over the past decades, physical architectures have changed from monolithic processing elements to networked computing resources of a heterogeneous nature. The growing divide between the increasing pluriformity in function and heterogeneity in physical architectures brings about an array of challenges for real-time system design. This presentation will highlight some of the developments in Model-Based Design of embedded systems and challenges in bridging the divide.

Bio:
Pieter J. Mosterman is a Senior Research Scientist at MathWorks in Natick, Massachusetts, where he works on computational modeling, simulation, and code generation technologies. He also holds an adjunct professor position at the School of Computer Science at McGill University. Prior to this, he was a research associate at the German Aerospace Center (DLR) in Oberpfaffenhofen. He earned his PhD in Electrical and Computer Engineering from Vanderbilt University in Nashville, Tennessee, and his M.Sc. in Electrical Engineering from the University of Twente, the Netherlands. His primary research interests are in Computer Automated Multiparadigm Modeling (CAMPaM) with principal applications in design automation, training systems, and fault detection, isolation, and reconfiguration. Dr. Mosterman designed the Electronics
Laboratory Simulator that was nominated for The Computerworld Smithsonian Award by Microsoft Corporation in 1994. In 2003, he was awarded the IMechE Donald Julius Groen Prize for his paper on the hybrid bond graph modeling and simulation environment HyBrSim. In 2009, he received the Distinguished Service Award of The Society for Modeling and Simulation International (SCS) for his services as editor in chief of SIMULATION: Transactions of SCS. Dr. Mosterman was guest editor for special issues on CAMPaM of SIMULATION, IEEE Transactions on Control Systems Technology, and ACM Transactions on Modeling and Computer Simulation. He has chaired over 30 scientific events, served on more than 100 international program committees, published over 100 peer reviewed papers, and is the inventor on over 80 awarded patents.
Title: Overview of Potential Software Solutions Making Multi-core Processors Predictable for Avionics Real-time Applications

Abstract:
Multicores are expected to be embedded in the next generation of avionics equipment, including Integrated Modular Avionics systems, Flight Control Units or cockpit display units. All these applications have a hard real time constraint that means they have to provide their service within predefined deadlines (a single miss will be considered as a fail).

WCET (Worst Case Execution Time) is key to ensure that a piece of software meets its deadline for each task. WCET can be either computed with dedicated tools or gathered through extensive measurements. WCET evaluation on multi-core processors is currently not measurable except if software if full mastered linked to the presence of interferences at hardware level, that occur when several cores use concurrently shared resources including main memory, shared caches and I/Os. A processor can be considered as predictable only when the impact of interferences on software’s execution time is bounded, so that a WCET can be evaluated. Several approaches have been investigated both by academic and industrial actors. They can be dispatched in two classes: deterministic hardware and deterministic software. Hardware solution consists in using a processor that is predictable by construction, for any embedded software. As far as we know no COTS solution has been developed yet. Software Solution allows to use the processor’s resources within a specific usage domain for which we know the processor is predictable. The presentation proposes a comparison of existing solutions that belong to this second category.

Bio:
An Engineer by background, he joined Thales in 1980 after graduating from ENSEEIHT1 University (Ecole Nationale Supérieure d’Electronique, Electrotechnique, Informatique et Hydraulique de Toulouse, France) with a master in Computing & Signal processing. A French national, he has worked in multiple locations and areas for Thales spanning 35 years career covering computing first in the naval domain for submarines, torpedoes and surface ships then in the aircraft military area for fighters and transport,
and now covering both commercial and military areas. Marc has spent five years as a Technical Director with the mission to be the Design Authority for all the projects and programs covering the domain of embedded computing. Now he manages the R&T at the Avionics Division Level; he is involved in advanced researches in this domain and has more than 38 publications and 17 patents in the area of sensors management, processing, modeling and recently in the analysis of ageing phenomena for components using DSM2 (Deep Sub Micronic) technologies. For certified commercial & military aircraft he has participated to the introduction of IMA3 (Integrated Modular Avionics) as the Avionics Computing Reference and now he is working on the preparation on the next generation of these systems. He is also the pilot for the Strategic Activity Domain (DAS) named Embedded System Software and Hardware (SE²L) within the Aerospace Valley cluster and the co-pilot for the DAS Photonics for Aeronautic and Space (PHAROS) within the Route Des Lasers Cluster.