Specialised Architecture of Dedicated Hardware Processors for Real-Time Image Data Pre-Processing

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1. A real time video system

Image processing algorithms can be conventionally divided into several levels. Algorithms of low level (I) image processing are typically performed as a sequence of simple operations such as a look-up-table, binarization, median filtering, convolution, logic operation and others. The middle level (II) image processing does image segmentation, object localisation, form recognizing and character form indication. High level image processing analyses complicated scenes: movement object detection and real-time object control. The high level (III) image processing generates algorithms and parameters for low and middle level image processing.

![Fig. 1. A real-time image processing levels](image)

The situation is very complicated when low level image processing operations are realised in hardware processors. Higher levels can require a change of operation realised by the dedicated hardware. Dedicated hardware processors application in a FPGA structure is a good solution in this situation. Dedicated hardware processors can be programmed by a Master Processor in the real-time mode.

2. Dedicated hardware processors

The conventional approach to the video image processing is connected with many data transfers between video memory buffer and microprocessors units. Therefore, eliminating time consuming transfers and applying a pipelined image processing system seems to be a valuable solution. This architecture particularly is a destination for low level image processing. Author designed and built a specialised pipelined multiprocessor architecture for specialised hardware processors. A special, custom pipeline bus standard was designed to provide a convinceable way of applying pipeline processors.

The author designed and built some dedicated hardware processors in FPGA structure: median filter, logic processor, look-up-table processor, convolution processor and histogrammer. Dedicated hardware processors implementation in the Xilinx FPGA used another chips: FIFO buffers and Triple Port RAM.

3. Conclusion

Presented in this paper are dedicated hardware processors implemented in a FPGA structure as this specialised pipelined architecture is very competitive to conventional computation. The pipelined multiprocessor architecture eliminated many time consuming data video transfers and a reconfigurable hardware allows a realization of different algorithms in the universal hardware.

Operation's times in the hardware processor are:

- look-up-table - 66 ns,
- median filtering - 68 μs,
- 3x3 convolution - 102 μs.

For comparison in the Data Translation dedicated modul DT2878 (DSP32C) the operation's time for 3x3 convolution is even 1180 ms. and for adding two frames is 250 ms. Another modul FT200 made by Alcron (two i860 processors) realises a 3x3 convolution in 51.9 ms.

The constructed pipelined multiprocessor unit for a fast image data pre-processing in real-time application was realised in the VME bus standard. It works with autonomous VME modules (CPU MC68030, local RAM, EPROM, I/O modules) running MICROWARE's real-time OS-9 operating system. Under development are system functions as well as a grafical user interface with MGR window graphic package.