Abstract
The research on 3D stacked IC (3D-SIC) technology has advanced to the point that virtually all semiconductor companies have now released or announced 3D-SIC products, or are developing such products in stealth mode. In 3D-SIC packages, multiple chip dies are stacked vertically, which results in a dense integration, possibly involving heterogeneous technologies, in an ultra-small footprint with considerable benefits for performance, power, and cost. In this presentation, we will introduce the main 3D-SIC components and build on those an ultra-short course on 3D stack architecting. The 3D benefits can only materialize if 3D-SICs can be properly tested for manufacturing defects. Recently, the test community has started to work on test solutions for these IC products, signaling that their high-volume market introduction is indeed imminent.

Biography
Erik Jan Marinissen is Principal Scientist at the world-renowned research institute imec in Leuven, Belgium, where he is responsible for the research on test and design-for-test, covering topics as diverse as TSV-based 3D-stacked ICs, silicon photonics, CMOS technology nodes below 10nm, and STT-MRAMs. In addition, he is Visiting Researcher at Eindhoven University of Technology, the Netherlands. Previously, he worked at NXP Semiconductors and Philips Research Laboratories in Eindhoven. Marinissen holds an MSc degree in Computing Science (1990) and a PDEng degree in Software Technology (1992), both from Eindhoven University of Technology. He is (co-)author of 250 journal and conference papers and (co-) inventor on fifteen granted US/EP patent families. Marinissen is recipient of the Most Significant Paper Awards at ITC 2008 and ITC 2010, Best Paper Awards at the Chrysler-Delco-Ford Automotive Electronics Reliability Workshop 1995 and the IEEE International Board Test Workshop 2002, the Most Inspirational Presentation Award at the IEEE Semiconductor Wafer Test Workshop 2013, the HiPEAC Tech Transfer Award 2015, and finalist for the National Instruments’ Engineering Impact Award 2017. He served as Editor-in-Chief of IEEE Std 1500 and as Founder and Chair (currently Vice-Chair) of the IEEE Std P1838 Working Group on 3D test access. Marinissen is founder of the workshops ‘Diagnostic Services in Network-on-Chips’ (DSNOC), DATE’s Friday 3D Integration, and the IEEE ‘International Workshop on Testing Three-Dimensional Integrated Circuits’
(3D-TEST). He has been Program Chair of DDECS 2002, ETS 2006, 3D-TEST 2009-15, and DATE 2013, and General Chair of ETW 2003, DSNOC 2007-08, 3DIW 2009-10, and serves on numerous conference committees, including ATS, DATE, ETS, ITC, ITC-Asia and VTS. He serves on the editorial boards of *IEEE Design & Test* and Springer’s *Journal of Electronic Testing: Theory and Applications*. During the span of his career, Marinissen has supervised 35 international MSc and PhD students. He is a Fellow of IEEE and Golden Core Member of Computer Society. Marinissen has presented invited keynote addresses at 3DIC, APCCAS, ATS, CICC, DATE, DDECS, DTIS, ISVLSI, NTF, SEMICON Japan, SEMICON Korea, VLSI-DAT, and VLSI-SOC.
The SiLago Method: Next Generation VLSI Architecture and Design Methods

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Abstract
The VLSI community faces two challenges that we propose to address with the SiLago Method. The first problem is the unsustainably large engineering cost of VLSI design that is suffocating innovation and introduction of new product categories that requires orders of magnitude greater computational and silicon efficiencies that can only be achieved by custom hardware design. This recipe goes against the current state-of-the-practice, the software centric accelerator rich platform based design style that has not only failed to reduce the engineering cost but also delivers sub-optimal designs and does not scale with technology trends.

As a solution, we propose raising the physical design platform from the present day boolean level standard cells to micro-architectural level SiLago (Silicon Large Grain Objects) blocks as the atomic physical design building blocks and introduce a grid based structured layout scheme as a new physical design discipline to compose arbitrary designs by abutting SiLago blocks to eliminate the logic and physical syntheses for the end user. We call this the SiLago method and show that it provides 2-3 orders more efficient synthesis from application level compared to the standard cell based commercial design flows with a modest loss in design quality.

The SiLago architecture enables time-division multiplexing of resources to dynamically create private execution partitions that allows near memory computation, predictable and composable systems and also fine grain power management systems.

The SiLago method also holds promise to solve the second problem of lowering the cost of making masks. This can be done because in the SiLago method, the mask becomes composable in terms of the component SiLago block masks. As there are finite number of SiLago block types that can have only a finite number of neighboring SiLago block types, it is possible to store as pre-determined patterns of the SiLago block types in a library that are corrected for all types of lithographic impairments. Masks for arbitrary SiLago designs can then be composed using these component SiLago block masks.
We are applying the SiLago method to some advanced high-performance applications like building custom supercomputers for real-time simulation of human-scale biologically plausible models of cortex. Such a custom supercomputer would take less than 2 kWs and when scaled to mice sized cortex would consume less 2 Watts. The SiLago method is also being used to design super-computers for bioinformatics applications using neural networks for use in clinical genomics.

**Biography**
Ahmed Hemani is Professor in Electronic Systems Design at School of ICT, KTH, Kista, Sweden. His current areas of research interests are massively parallel architectures and design methods and their applications to scientific computing and autonomous embedded systems inspired by brain. In past he has contributed to high-level synthesis – his doctoral thesis was the basis for the first high-level synthesis product introduced by Cadence called visual architect. He has also pioneered the Networks-on-chip concept and has contributed to clocking and low power architectures and design methods. He has extensively worked in industry including National Semiconductors, ABB, Ericsson, Philips Semiconductors, Newlogic. He has also been part of three start-ups.