A WSI Hypercube Design Using Shift Channels

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Abstract

A novel design of a hypercube network (HC) on WSI (Wafer Scale Integration) is proposed. The design makes both static and dynamic reconfigurations feasible. A WSI HC design by applying the Diogenes method to a planar structure was proposed before. However, in Diogenes method, every time a wire passes a processing element (PE), it passes at least one FET. Therefore, the design has a drawback that there are many FETs in a link between PEs and then it brings a large communication delay time. The design proposed here reduces the number of FETs in a link between PEs by utilizing two channels, called shift channel and basic channel, for reconfiguration. The design can be accomplished by using a structure in which FETs are contained only in shift channels but not in basic channels. The channel is a bundle of wires which has a track width sufficient to make sub-HCs. A switch in the shift channel is similar to the switch of Diogenes method, but it is newly designed as a dedicated one.

1. Introduction

Researches on massive and parallel processing are in progress [1]-[3], while techniques on WSI (wafer scale integration), which build a large parallel system on a wafer, have been actively studied [4]-[8]. As a large number of processing elements (PES) are integrated on a wafer in WSI, the probability that defective PEs or defective wiring lines are included in the wafer is very high. Therefore, a design method overcoming such defects should be exploited for the practical WSI realization. Most of the studies on WSI have been for grid structures with small distance between PEs, for pipeline processing structures, and for systolic array structures [6]. Other systems or structures such as memory [10], neural net [11], tree [5],[9],[12], and cube [13]-[17] have also been studied.

A novel WSI hypercube (HC) design will be proposed in this paper, although it is theoretical yet. A WSI HC design by applying the Diogenes method [9] to a planar structure was proposed before [13]. One of the advantages in Diogenes method is that it is useful for both static and dynamic (run-time) reconfigurations which are desirable properties in practical WSI realization, considering maintenance in run time. However, in Diogenes method, every time a wire passes a processing element (PE), the wire passes at least one FET. Therefore, the design has a drawback that there are many FETs in a link between PEs and then it brings a large communication delay time. Another WSI HC design [14] is one using channels called basic channel which is a bundle...
of wires running parallel on a wafer, making a network. In the design, switches or devices for reconfiguration are not specified in particular, and almost all connections between a pair of wiring lines, which cross in horizontal and vertical channels in two different layers, are assumed to be possible. If dynamic reconfiguration is assumed in the design, extremely large number of switches or devices will be necessary for all cross points, which is not practical. Therefore, the design is not suited for the dynamic reconfiguration, that is, it is suited only for a static reconfiguration based on laser program, mask process, and so on [4],[5].

The proposed design reduces the number of FETs (switch devices) in a link between PEs by utilizing two channels, called shift channel and basic channel. The design preserves the structure which makes both static and dynamic reconfigurations possible. That can be accomplished by using a structure in which FETs are contained only in shift channels but not in basic channels, where the basic channel is almost the same as the conventional one [14]. A switch in the shift channel is similar to the switch of Diogenes method [9], but it is newly designed as a dedicated one. The proposed design will be evaluated by comparing it with the conventional method [13], which has the same reconfiguration scheme in the point of view of making both static and dynamic reconfigurations possible. The parameters maximum number of FETs in a link, distance between PEs, necessary array size, and construction probability will be derived for both designs in the same conditions and they will be compared. As a result, it can be said that the proposed design is superior to the conventional design.

As described later in section 5, the method proposed in this paper is called \((h,v)\) divided design. The \((1,1)\) divided design \((h=v=1)\) is the basis for the design of any \((h,v)\) divided design. Therefore, the \((1,1)\) divided design will be presented in detail from section 2 to section 4.

2. Layout structure

In this section, an outline of the proposed HC layout will be presented. Let \(d\) assume the dimension of a target HC. An array of processing elements (PE) consists of \(2q+t\) rows and \(2P+s\) columns on a wafer \((p=q=d)\), where \(p\) (\(q\)) is the dimension of the row network, RN, (column network, CN), which is a sub-HC of the HC, and \(t\) (\(s\)) is the number of redundant rows (columns). Figure 1 shows an outline of the proposed HC layout. Each square denotes a PE. There are \(p+q\) I/O ports on every PE for the constructions of RN and CN. There are two bundles.
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of wiring lines RBC\(_i\) (0 ≤ \(i ≤ 2^p-1\)) and RSC\(_j\) (0 ≤ \(j ≤ 2^q-1\)) called row basic channel and row shift channel, respectively, between adjacent PE rows, and also CBC\(_i\) (0 ≤ \(i ≤ 2^p-1\)) and CSC\(_j\) (0 ≤ \(j ≤ 2^q-1\)) called column basic channel and column shift channel, respectively, between adjacent PE columns.

RBC\(_i\) (CBC\(_i\)) is the same channel as the conventional one [14] which has the wire tracks necessary for constructing a one-dimensional HC array with 2\(^p\) (2\(^q\)) PEs. Figure 2 shows an example of the track usage of the row basic channel for the one-dimensional HC array with 2\(^p\) PEs (~3). The k-th point from the left (top) in RBC\(_i\) (CBC\(_i\)) connected to PE\(_k\) is called the k-th PE port of RBC\(_i\) (CBC\(_i\)).

In this paper, only PE's defect will be assumed. After all elements and components are fabricated on a wafer and PEs are tested, all switches in RSC\(_j\) and CSC\(_j\) are set to either normal mode or pass mode based on the PE's defect pattern on a wafer. These modes specify the connections among data lines on switches. By those switch establishments, necessary connections among PEs can be obtained and the HC construction is completed. Note that there are no programmed switches in any other part of the wafer, except RSC\(_j\) and CSC\(_j\).

3. Shift channel

3.1 Structure of a shift channel

The structure of a row shift channel RSC\(_j\) (0 ≤ \(j ≤ 2^q-1\)) will be presented here. The structure of a column shift channel CSC\(_j\) (0 ≤ \(j ≤ 2^q-1\)) is similar to that of the row shift channel. Figure 3 shows an example of an RSC\(_j\). SW\(_{ij}\) is a switch called a shift switch, and D\(_{ij}\) and D\(_{sij}\) are terminals for \(d (= p+q)\) links. But, there are no D\(_{sij}\) in the rightmost s SW\(_{ij}\) (2\(^p\) S\(_{j-1}\)). The s links and s control lines run parallel in RSC\(_j\). Figure 4 shows an example of the connections of D\(_{ij}\) links, and D\(_{sij}\) in RSC\(_j\). If necessary, links are shifted at switches as shown in the figure. D\(_{ij}\) is not connected at SW\(_{ij}\) marked " • " and by this mechanism, a defective PE is separated from the HC network.

SW\(_{ij}\) consists of SWC\(_{ij}\) and CC\(_{ij}\) as shown in Fig. 5 (a). SWC\(_{ij}\) is a switching circuit for data links and CC\(_{ij}\) is a control signal generator for SWC\(_{ij}\). B\(_{ij}\) (B\(_{ji}\)) are s bidirectional data links connected with SW\(_{ij}\) (SW\(_{ji}\)). C\(_{ij}\) (C\(_{ji}\)) are s control lines receiving from SW\(_{ij}\) (sending to SW\(_{ji}\)). SWC\(_{ij}\) and CC\(_{ij}\) of s=4 are shown in Fig. 5 (b) and Fig. 5 (c), respectively. A data link is represented by a bit line in the figure. Note that, in the proposed design, any link passes only one FET every time it passes one SW\(_{ij}\).

There is a fuse F\(_{ij}\) in CC\(_{ij}\). SW\(_{ij}\) is set to the pass mode if and only if the fuse F\(_{ij}\) is cut off. All F\(_{ij}\) in shift switches may be located together in some area in the wafer, or equivalent information to F\(_{ij}\) may be given by programmed ROM located somewhere in the wafer. The k control lines from bottom in CC\(_{ij}\) have logical value 1, if and only if there are k pass mode switches in the left side of SW\(_{ij}\). For example, if there are two pass mode switches in the left side of SW\(_{ij}\), then C\(_{ij,10}\) = C\(_{ij,11}\) = 1, C\(_{ij,12}\) = C\(_{ij,13}\) = 0.
Fig. 3 An example of an RSC $\beta=3, s=4$.

Fig. 4 An example of the connections of RSC $\beta=3, s=4$.

(a) SW$_{ij}$.

(b) SWC$_j$ ($s=4$).

(c) CC$_j$ ($s=4$).

Fig. 5 Shift switch.
3.2 Function of shift switch

The shift switch SW<sub>i</sub> is set to either normal mode or pass mode. The function of the modes are as follows.

(a) normal mode: In Fig. 4, the switches SW<sub>i</sub> without the mark "·" are in this mode. D<sub>5</sub> is directly connected to D<sub>5</sub> or to the topmost effective link in the right side of SW<sub>i</sub>. And also, effective links in the left side of SW<sub>i</sub> are connected to the right side links by shifting one link downward. In this case, the bottommost link in the left side is connected to D<sub>5</sub>. (b) pass mode: In Fig. 4, the switches SW<sub>i</sub> with the mark "·" are in this mode. Effective links in the left side of SW<sub>i</sub> are connected to the right side links as they are. And also, D<sub>5</sub> is connected to the topmost effective link in the right side of SW<sub>i</sub>. D<sub>5</sub> remains open.

4. Network construction algorithm

An outline of HC network construction algorithm will be presented here. This algorithm decides all switches' modes. As the total number of redundant PEs in a row (column) is s (t), the number of pass mode switches in an RSC (CSC) is at most s (t). The algorithm makes an HC construction probability (it is also called survivability[7]) as high as possible within the restriction of the number of pass mode switches. The algorithm consists of two steps which are called row direction's shifts (Step 1) and column direction's shifts (Step 2). Step 1 is carried out first, and Step 2 is carried out using the result of Step 1. The switches' modes after Step 1 and Step 2 determine the correspondence from physical PE addresses to logical PE addresses. Let PE<sub>i</sub> (PE<sub>ij</sub>) denote physical (logical) PE address in physical row i and physical column j (logical row k and logical column l). If and only if PE<sub>ij</sub> corresponds to PE<sub>il</sub>, PE<sub>ij</sub> is connected to the i-th PE port in RBC<sub>k</sub> and the k-th port in CBC<sub>l</sub> through RSC<sub>i</sub> and CSC<sub>i</sub>. Note that each PE must be connected with d (=p+q) links through PE's ports, and the first p links (the later q links) must be connected to RBC (CBC) for constructing RN (CN). Therefore, PE<sub>ij</sub> reaches to the i-th PE port in RBC<sub>k</sub> and the k-th PE port in CBC<sub>l</sub> as follows: PE<sub>ij</sub>→(D<sub>5</sub> in RSC<sub>i</sub>)→RSC<sub>i</sub>→(D<sub>5</sub> in CSC<sub>i</sub>)→CSC<sub>i</sub>→(D<sub>5</sub> in CSC<sub>i</sub>)→(the i-th PE port in RBC<sub>k</sub> and the k-th PE port in CBC<sub>l</sub>). Therefore, Step 1 and Step 2 specify all connections between used good PEs and PE ports in RBC and CBC. For simplicity, let us assume that p=q. The case of p≠q is similar to that of p=q.

The row direction's shift (Step 1) is carried out by checking in every column if a certain condition is satisfied:

Step 1: row direction's shift

Every PE's row direction's shift is carried out by setting at most s shift switches in a row shift channel RSC<sub>i</sub> (0≤i≤2s+t) to the pass mode. A shift switch without setting remains in the normal mode. In this case, N<sub>TAIL</sub>≤t must be satisfied for every column j (0≤j≤2t-1), where N<sub>TAIL</sub> is the total number of defective PEs connected electrically to D<sub>5</sub> terminals of SW<sub>i</sub> (0≤k≤2s+t) in the column shift channel CSC<sub>j</sub>. If this condition is not satisfied, the HC construction fails.

Step 2: column direction's shift

At most t SW<sub>ij</sub> (0≤i≤2s+t) in a CSC<sub>j</sub> in which D<sub>5</sub> are connected electrically to defective PEs, are set to the pass mode. (Step 2 always succeeds, since the number of such D<sub>5</sub> connecting to defective PEs in a CSC<sub>j</sub> is less than or equal to t for all j after Step 1 succeeds.)

Figure 6 shows an example of applying the algorithm to the case of p=q=2, s=t=1. In Fig.s 6 (a) and (b), CSC<sub>j</sub> are omitted, and in Fig.s 6 (c) and (d), RSC<sub>i</sub> are omitted. Figure 6 (a) shows the initial switch connections in RSC<sub>i</sub> (0≤i≤4), where all switches are in the normal mode. Each address attached to each terminal shows a physical PE address which is connected to the
Figure 6 (b) shows the switch connections in $\text{RSC}_i (0 \leq i \leq 4)$ after Step 1 is carried out. Figure 6 (c) shows the initial switch connections in $\text{CSC}_j (0 \leq j \leq 3)$. As $D_{si}$ in $\text{RSC}_i$ is directly connected to $D_{sj}$ in $\text{CSC}_j$, the address attached to $D_{si}$ in Fig. 6 (c) is the same as the one of $D_{sj}$ in Fig. 6 (b). Figure 6 (d) shows the switch connections in $\text{CSC}_j (0 \leq j \leq 3)$ after Step 2 is carried out. As a result, the algorithm succeeds in constructing the HC with the restriction of $s = t = 1$. Figure 6 (e) shows the result, where the logical addresses are shown in the effective PEs used.

![Switch connections](image)

**Fig. 6** An example of applying the algorithm $(p=q=2, s=t=1)$.

### 5. The $(h,v)$ divided design

In the $(h,v)$ divided design, a total HC PE array is divided into $h$ sets of PE columns and $v$ sets of PE rows. That is, the PE array is divided into $h \times v$ PE sub-arrays, called blocks. All blocks have the same structure. The block consists of $(2h+v)h$ PE rows and $(2v+s)h$ PE columns. In a block, there are $s$ redundant PEs in a row and $v$ redundant PEs in a column.

Each block can be constructed by using row and column shift channels in the block. However, the row (column) basic channel $\text{RBC}_i$ ($\text{CBC}_j$) is not divided. If all blocks succeed in constructing sub-HCs, then the total HC construction succeeds. Each block design is the same as the $(1,1)$ divided design presented from section 2 to section 4.

Figure 7 shows an HC array using the $(2,2)$ divided design $(p=q=3, s=t=2)$. In each block, a $4 \times 4$ PE array can be constructed from a $5 \times 5$ PE array. An HC for $d=6$ can be constructed by using $2 \times 2$ blocks. This design is similar to the design called patching method [18].
6. Design evaluation

In this section, the proposed design will be evaluated by comparing it with the conventional method [13], which has the same reconfiguration scheme in the point of view of making both static and dynamic reconfigurations possible. There are two similar designs called DSIRN and DSRN in reference [13]. However, as DSIRN is superior to DSRN, DSIRN will be taken for the comparison. The parameters of the maximum number of FETs in a link (denoted by \( N_p \)), the distance between PEs (\( D \)), the necessary array size (\( S \)), and the construction probability (\( P \)) will be derived for both designs in the same conditions (or some of the results in reference [13] will be utilized) and they will be compared. As a result, it can be said that the proposed design is superior to the conventional design. We assume here HCs with \( p=q \) for simplicity.

6.1 Number of FETs in a link and distance between PEs

Let the PE be a square of unit width and height. Assume that the width of wiring area can be ignored here (Let us assume the same condition as in reference [13] for comparison). Let \( N_{p(h,v)} \) and \( D_{(h,v)} \) denote \( N_p \) and \( D \), respectively, in the proposed \((h,v)\) divided design. They are derived as follows.

\[
N_{p(h,v)} = 2[(sh) + (t/v) + 2],
\]

\[
D_{(h,v)} = 2^{(h)} + 2[(sh) + (1/v) + s/2], \quad s \geq t.
\]

It is remarkable that \( N_{p(h,v)} \) is independent of the dimension of the target HC.

Let \( N_{p0} \) and \( D_{0} \) denote \( N_p \) and \( D \), respectively, in DSIRN. They have been derived as follows [13].
Figures 8 and 9 show $N_F$ and $D$ of $p=q=5$ for redundant degree ($R$), respectively, where $R = (the\ total\ number\ of\ redundant\ PEs)/2^d$. For your information, Fig. 9 also shows $D_{01}$, which is obtained from the design in reference [14]. Graphs for other values of $p$ and $q$ are similar to those of Fig. 8 and 9. The following statements can be made from the graphs.

1. $N_F(h,v)$ is smaller than $N_{01}$. If $h$ and $v$ are larger, the difference is greater.
2. $D(h,v)$ with small values of $h$ and $v$ (for example $h=v=1$) is larger than $D_{01}$. However, for larger values of $h$ and $v$, $D(h,v)$ is similar to or smaller than $D_{01}$ (for example $h=v=4$).

6.2 Array size

Let the width of a link connecting two PEs be unit, and the width of PE be $w$ (PE is square). Let $N_F(N_{01})$ be the width (the number of tracks) of a basic channel necessary for constructing a one-dimensional HC array of $p$ ($q$) dimension [14]. Let $W_{(h,v)}$ and $H_{(h,v)}$ denote the width and height of an array using the $(h,v)$ divided design. They can be represented as follows.

$W_{(h,v)} = (w+s+h+d+N_{01})2^d + w$,
$H_{(h,v)} = (w+s/h+d+N_{01})2^{d+1}/h + d/1$.

Array size, denoted by $S_{(h,v)}$, is derived as follows.

$S_{(h,v)} = [W_{(h,v)}H_{(h,v)}] = [(w+s/h+d+N_{01})2^{d+1}/h + d/1]$. On the other hand, the array size of DSRN, denoted by $S_{01}$, is given as follows [13].

$S_{01} = [(w+s/h+1)(2^d+s)] = [(w+2^d/s)(2+s)/2^d]$. $S_{(h,v)}$ and $S_{01}$ will be compared numerically. The following items will be assumed for simplicity.

1. $p=q$, $d = 4, 6, 8, 10, 12$.
2. A link consists of $8$ data bits and $4$ control bits.
(3) The wire width and the space width between adjacent wires are both 1 \( \mu \)m.
(4) The width \( w \) of PE (PE is square) is 0.5cm or 1cm.
(5) All FETs for switching and control can be embedded into the wiring area.

Figures 10 (a) and (b) show the relation between \( S \) and \( R \) for \( p=q=5, w=0.5 \text{cm} \), and for \( p=q=5, w=1.0 \text{cm} \), respectively. For your information, the graphs also show \( S_{01} \), which is obtained from the design in reference [14]. Graphs of other values of \( p \) and \( q \) are similar to those of Fig.s 10 (a) and (b). As a result, \( S_{01} \) is smaller than \( S_{02} \). For example, \( S_{01}(h,v) \) is about 70% of \( S_{01} \) in case of \( p=q=5, w=0.5 \text{cm}, R=0.5 \).

### 6.3 Construction probability

Construction probability (survivability [7]) is a probability that a target \( d \)-dimensional HC can be constructed on a wafer. The probabilities of the proposed design and conventional design (DSRN) will be derived and compared. Let \( P_{A}(\rho) \) and \( P_{B}(\rho) \) denote them, where \( \rho \) is called spare demand and defined as follows.

\[
\rho = \frac{\text{the total number of defect PEs}}{\text{the total number of redundant PEs}}
\]

\( P_{A}(\rho) \) and \( P_{B}(\rho) \) are derived in a way similar to that in reference [14], that is, using computer simulation, under the condition that defective PEs appear randomly.

Figures 11 (a) and (b) show \( P_{A}(\rho) \) and \( P_{B}(\rho) \) for \( p=q=5, R=0.129 \) and \( p=q=5, R=0.563 \), respectively. For your information, the graphs also show \( P_{01}(\rho) \) and \( P_{02}(\rho) \) obtained from DSRN in reference [13] and the design in reference [14], respectively. Graphs for other values of \( p \) and \( q \) are similar to those. As a result, \( P_{A}(\rho) \) is greater than \( P_{B}(\rho) \) for small values of \( h \) and \( v \). However, \( P_{A}(\rho) \) is smaller than \( P_{B}(\rho) \) for larger values of \( h \) and \( v \); for example, \((h,v)=(8,8)\) in case of \( R=0.563 \).
7. Conclusion

A novel WSI HC design using shift channels, called $(h,v)$ divided design, was presented for the purpose of reducing the number of FETs in a link between PEs. The design can be accomplished by making an array structure so that FETs are contained only in shift channels but not in basic channels. The design preserves the structure which makes both static and dynamic reconfigurations possible.

The proposed design was compared to the conventional design using 4 parameters, which are the number of FETs in a link between PEs, distance between PEs, array size, and construction probability. As a result, it can be said that the proposed design, with a relatively small number of divisions, is superior to the conventional design.

A detailed design for a practical implementation, and a defect tolerant design for defects in wires and switches in channels are left for future works.

References