Abstract

This paper describes an implementation of chip built-in self-test using by-pass boundary scan design. This basic structure is then modified to implement a universal self-test structure for cards, boxes and systems.

Objective

To reduce the cost of testing digital circuits, self-test methods have been widely used by logic designers during the last decade, especially, at the chip level. Built-in self-test (BIST) methods (1,2,3,4) that integrate additional test circuitry with original design and built-out self-test methods (5,6) that place test circuitry in the tester have been extensively studied. However, these self-test methods are aimed at chip and module tests only. The objective of this paper is to describe a technique that implements a universal self-test structure. This self-test structure uses a by-pass boundary scan technique to minimize overhead in silicon and delays caused by data selection.

Descriptions of STUMP self-test structure

Figure 1 depicts the self-test structure of a conventional LSSD chip that follows the STUMP approach (1). A parallel random pattern generator (PRPG) generates flat-random test patterns. These random patterns are decoupled before feeding the LSSD scan chains. A multiple-input signature register (MISR) collects output...
responses of the logic circuits under test through multiple scan rings. A detailed implementation of this circuit is described in the paper co-authored by P. Bardell et al. (1).

To test boundary logic depicted in Figure 1, input and output boundary scan latches are required. In addition, a multiplexer is needed to select data either from a functional or test input. Additional delay is added to the signal path due to the usage of this multiplexer. In many cases, minimization of this delay is critical to a competitive design.

Another drawback of this structure is that even if boundary latches are used, there is no easy solution to extend this structure to the higher level self-tests.

Descriptions of by-pass boundary scan design

In this paper, a chip self-test structure for higher level self-test is shown in Figure 2. This structure assumes all primary input pins are also the primary input pins of cards. Figure 2 shows an input logic circuit 'A' feeding a LSSD scan chain S1. The output of S1 feeds another logic group B and the output of B feeds another scan chain S2. The number of logic group and scan chains is determined by the circuit designers. Instead of feeding the primary inputs with external applied random patterns or internal random patterns supplied by boundary scan latches, a series of random patterns are applied by the outputs of scan latches S1 or S2 or Sn (depend on the wirability) and feed into a tri-state gate T. If the output of the logic macro C is "1", tri-state gate T is disabled and the enable-pin of the receiver R is active, the input logic circuits A receives the signals from the incoming chips. The output of the macro block C is determined by three inputs: BOUNDARY, LEVEL and SYSTEM MODE. If the BOUNDARY pin is at a logical state of '1', it means the
The state of the LEVEL pin indicates the level of self-test. If LEVEL is '00', it is at chip self-test level. If LEVEL is '01', it is at card self-test level. If LEVEL is '10', it is at box self-test level. And if LEVEL 's '11', it is at system self-test level.

The SYSTEM_MODE input pin of macro C indicates if the system is at a functional mode or self-test mode. If SYSTEM_MODE is '1', all of the self-test circuits are disabled. If SYSTEM_MODE is '0', it is at one of the self-test modes.

A second version of the modified chip self-test structure is shown in Figure 2b. An additional set of macro logic C and tri-state logic is used for a different design case. In this design, some of the primary input pins are located at the boundary of the cards (or boxes or systems) and others are located within the unit under test. Different values are assigned to the BOUNDARY pins dependent of their locations.

Description of higher-level self-test

Figure 3 depicts an example of a card self-test structure. The PIs of chip 1 are all boundary pins of the card under test and, therefore, BOUNDARY is set to '1' and LEVEL is set to '01' for card self-test. The outputs a, b, c of chip 1 are connected to the inputs of chip 2, and the BOUNDARY pin that controls these inputs is set to '0' (to indicate internal pins). While the primary input pin d shown in chip 2 is a boundary pin of the card under test, therefore, the BOUNDARY pin is set to '1'.

This structure can be extended to the box and system self-test. Figure 4 explains the overall principle of operation. Macro C, as described before, has three inputs
which enable the appropriate level of self-test.

1. SYSTEM MODE - configures the circuit into a self-test mode or a functional mode.

2. BOUNDARY - Once in self-test mode, the signal configures the circuit into either accepting data from the primary inputs or from the internally generated self-test patterns. These internally generated patterns are fed back from the registers through a tri-state pass gate back onto the outputs of the primary input receivers. A boundary-pin of a lower-level self-test could become a non-boundary-pin of a higher-level self-test.

3. LEVEL - This two-strand net configures the circuit into either a chip, card, box or system level self-test. For example, chip self-test has a level 00 and card self-test has a level 01, etc.

Based on these signals, logic 'MACRO C' can enable the chip, card, box and system to be at different levels of self-test. The signature registers that are not shown in the figure are also configured according to the level of self-test. This paper allows the flexibility for different levels of self-test. A chip, card, box or system can be a boundary where it generates its own self-test patterns or accepts patterns from another chip, card, box, or system of various levels of self-test configurations.

References:


Figure 1: Self-test structure of STUMP
Figure 2: Modified chip self-test structure for higher-level tests
Figure 2b  Second version of modified chip self test structure
Figure 3: Card self test structure
Figure 4: A universal self-test structure.