A METHOD FOR THE CONSISTENT REPORTING OF FAULT COVERAGE

Warren H. Debany & Kevin A. Kwiat
Rome Laboratory, RL/ERDA
Microelectronics Reliability
Griffiss AFB NY 13441

Sami A. Al-Arian
University of South Florida
Computer Science & Eng.
Tampa FL 33620

Abstract

A standard procedure has been developed for fault coverage measurement. Procedure 5012 of MIL-STD-883 governs the reporting of fault coverage for digital microcircuits for military applications. It describes requirements for the development of the logic model for an IC, fault universe, fault simulation, and reporting of results. Procedure 5012 provides a consistent means of measuring fault coverage for an integrated circuit regardless of the specific logic and fault simulator used. It addresses the testing of complex, embedded structures that are not implemented in terms of logic gates, such as RAMs, ROMs, and PLAs. Fault coverages for gate-level and non-gate-level structures are weighted by transistor counts to arrive at an overall fault coverage value. The procedure addresses built-in-self-test based on the use of linear feedback shift registers for output data compaction. Two fault sampling procedures are permitted. A Fault Simulation Report documents the fault coverage level obtained, as well as the assumptions, approximations, and methods used.

Discrepancies Between Fault Simulators

Nearly all DoD contracts that involve digital logic testing include fault coverage-related requirements. These may include minimum acceptable levels of fault coverage, or simply the requirement that fault coverage must be measured and reported. It is difficult to reconcile the results from various stages of test program set (TPS) development and item testing when different fault grading procedures and tools are applied at the microcircuit level and every subsequent level of assembly. Frequently, several TPSs are developed independently for the same chip, board, or module. It is common to observe differences of as much as 30 percentage points between fault coverages obtained for the same TPS by two different fault simulators.

A study performed by the University of South Florida (USF) investigated the specific reasons why such large differences in reported fault coverage occur [1][2]. Based in part on this study, a military test method has been developed that provides guidance to the engineers who develop the logic models and use fault grading tools so that consistent results can be obtained. This paper outlines the major points of MIL-STD-883 Procedure 5012 [3][4], "Fault Coverage Measurement for Digital Microcircuits," which specifies the methods by which fault coverage is reported for a test applied to an integrated circuit (IC).

Standard Procedure For Measuring Fault Coverage

In order to simulate sequential digital logic, at a minimum the logic states zero (0), one (1), high-impedance (Z), and unknown (X) must be supported in at least unit-delay, event-
directed simulation. The initial state of all memory elements must be X.

Assuming that the Automatic Test Equipment (ATE) does not directly measure for the Z state on an output, a hard detection is where there is a 0/1 or 1/0 difference between the outputs of the fault-free and faulty models of the device-under-test (DUT). A potential detection is where the fault-free output is 0 or 1, and the faulty output is Z or X. Credit is awarded for fault detection if the fault causes a hard detection. Credit is not awarded for potential detection only, unless it is shown that the potential detection implies hard detection (as is the case with most clock line faults).

Models are composed of gate logic (G-logic) and block logic (B-logic). G-logic consists of simple components and their interconnections. Examples of simple components are the indivisible primitives generally understood by simulators, such as logic gates and flip-flops. More complex components are referred to as B-logic. Examples of B-logic components are RAMs, ROMs, and PLAs (even if they are built into the simulator), and user-defined behavioral models. B-logic is usually treated as a "black-box" for the purpose of fault simulation, and faulting is limited to the inputs and outputs of the blocks. The logic model is divided into non-overlapping partitions of G-logic and B-logic.

For G-logic, the fault universe consists of fault equivalence classes of the single stuck-at-zero and stuck-at-one faults on the logic lines in the model of the DUT. It is impractical at this time to require the determination of fault coverage on any other basis such as shorts, opens, pattern-sensitivity, and transient and multiple faults. A major finding of the USF study was that the most effective method of reducing the differences between fault simulators is to report coverage in terms of fault equivalence classes. It is sufficient to use simple, structurally-based fault equivalencing rules to generate the representative faults for the fault equivalence classes. Undetectable faults are permitted (but not required) to be dropped from the set of faults considered.

No specific fault model is associated with B-logic. An "established test algorithm" must be used to test each B-logic component or B-logic partition; otherwise, the fault coverage for that partition is reported as 0%. A test algorithm is considered to be "established" if, for instance, it has been published and is in common use with demonstrably useful results, or if data are available that apply to a particular case. An example is where a RAM is tested using a standard algorithm with known effectiveness.

Built-in-self-test structures based on linear-feedback shift registers (LFSRs) are allowed to be fault-graded without the LFSR and the resulting fault coverage for the block to be reported for the block, minus a penalty value based on the length of the LFSR. The penalty values, based on experiments performed with a variety of circuit types and LFSR polynomials, represent the worst-case probabilities of aliasing for the types of errors that occur in the presence of logical faults in digital circuits. If C is the measured fault coverage of a logic block (excluding consideration of the LFSR) then the reported fault coverage is \((1 - p)C\), where p is a function of the degree of the LFSR polynomial as specified in Table 1. It is required that the LFSR implement a primitive polynomial.

Simulation of all faults in the fault universe may not be practical in some situations due to its size, or because of tool limitations. Fault sampling is where the reported fault coverage is based on simulation of only a randomly-selected subset of the fault universe. A lower bound on the fault coverage in a G-logic partition can be estimated using a fixed sample size. Table 2 lists penalty parameters \(r\) and the corresponding fault sample sizes \(n\). For example, let the penalty \(r = 0.02\) be selected. The corresponding value of \(n\) is 1,740. The
Table 1. Penalty values \( p \) for LFSR signature analyzers implementing primitive polynomial of degree \( k \).

<table>
<thead>
<tr>
<th>Degree ( k )</th>
<th>Penalty value ( p )</th>
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</thead>
<tbody>
<tr>
<td>( k &lt; 8 )</td>
<td>1.0</td>
</tr>
<tr>
<td>( 8 \leq k \leq 15 )</td>
<td>0.05</td>
</tr>
<tr>
<td>( 16 \leq k \leq 23 )</td>
<td>0.01</td>
</tr>
<tr>
<td>( 23 &lt; k )</td>
<td>0.0</td>
</tr>
</tbody>
</table>

Table 2. Sample sizes used to obtain lower bound on fault coverage using Fault Simulation Procedure 2.

<table>
<thead>
<tr>
<th>Penalty value ( r )</th>
<th>Min. Sample Size ( n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>6860</td>
</tr>
<tr>
<td>0.015</td>
<td>3070</td>
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<tr>
<td>0.02</td>
<td>1740</td>
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<tr>
<td>0.03</td>
<td>790</td>
</tr>
<tr>
<td>0.04</td>
<td>450</td>
</tr>
<tr>
<td>0.05</td>
<td>290</td>
</tr>
</tbody>
</table>

A set of 1,740 faults is simulated, and suppose that the number of hard detections \( d \) is found to be 1,679. Then the reported fault coverage is \( \frac{d}{n} - r = \frac{1,679}{1,740} - 0.02 = 94.49\% \). A second fault sampling procedure accepts or rejects a claimed lower bound on fault coverage in a G-logic partition using a fixed sample size.

The overall fault coverage is given by \( F = \sum \frac{F_i}{T_i} \), where \( m \) is the number of logic partitions, \( F_i \) is the fault coverage of the \( i^{th} \) partition, and \( T_i \) is the fraction of transistors contained that partition.

**Fault Simulation Report**

The applicable procurement document may contain guidelines, goals, or requirements for the level of fault coverage that should be obtained, selection of random samples of faults, or restrictions on test algorithms for structures such as RAMs. In response, the reported fault coverage is supported by a Fault Simulation Report. The Fault Simulation Report addresses the following items:

a. Statement of the overall fault coverage.
b. Description of logic partitions.
c. Description of B-logic test algorithms and how they were applied.
d. Justification for any initial condition, other than X, for any memory element.
e. Justification for any approximations used, including estimates of fault coverages, transistor fractions, and counts of undetectable faults.
f. Description of the fault equivalencing procedure used, if unique.
g. Justification for declaring any fault to be undetectable.
h. If the test vector sequence is formatted differently between the ATE and the fault
simulator, justification that fault coverage achieved on the ATE is not lower than that reported.
i. Justification of the use of fault simulation based on fault sampling.
j. If fault sampling is used, method of obtaining random fault sample.
k. In the event that a test technique or design-for-testability approach is used that provides additional control or observation test points beyond those provided by the DUT's primary inputs and primary outputs (by means of an internal access technique such as scan design, \( I_{DDQ} \) [5], or "CrossCheck" [6]), justification that the stated fault coverage is valid.

Implementation Progress

In 1987 the general requirements now detailed in 5012 were first made part of MIL-STD-454L Requirement 64. The current version of Requirement 64 and the MIL-M-38510 detail specifications (JAN "slash sheets") for bipolar and CMOS gate arrays, and MIL-M-38535 (Qualified Manufacturers List) now reference 5012.

It is possible to meet the requirements of 5012 without having available a fault simulation package that directly supports it. Modeling workarounds and manual calculations can be used, and preprocessors and postprocessors can be developed to obtain results in accordance with 5012. The procedure expressly permits noncompliant methods to be used so long as their use is clearly documented, and estimates are provided as to how much of a difference is expected to be present in the results. TI's Defense Systems & Electronics Group has documented the use of 5012 in grading a test program set for an application-specific IC for signal processing [7].

References