CURRENT-MODE TECHNIQUES
FOR ANALOG VLSI: TECHNOLOGY AND
DEFECT TOLERANCE ISSUES

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Abstract
Future large scale analog computational systems will have to cope with manufacturing defects and mismatch in individual components. We argue that current-mode design techniques, and in particular minimal designs at the transistor level are consistent with future manufacturing requirements for wafer scale analog systems.

1 Introduction
Analog VLSI is an emerging technology aimed at increasing the computational power of present day computers [Me89]. This notion of large scale analog or quasi-analog computation is motivated by known principles and organization of information processing in biological neural systems. Aside from using this new technology as a modeling tool it is believed that useful systems will be manufactured on a large scale and will augment present day digital signal/pattern processing systems [Mego].

A common thread in these emerging systems is an effective and efficient use of actual physical space. Thus, the notion of geometric computation can be introduced. Hamming distance classifiers and associative/heteroassociative memories [Bo89a, Bo89b] as well as other systems that involve different distance norms, belong to this category. A different class of geometric processors involve local connectivity and resistive or diffusive networks aimed primarily at solving problems in computer vision [Me89, CK89, An91, BoAn91].

All the above have the potential for wafer scale integration. However unlike digital VLSI systems that can have large physical sections idle, massively parallel analog VLSI systems are always computing. Therefore energy consumption in sub-systems should be constrained and devices should be operated at small current levels, often in sub-threshold/transition region. To achieve VLSI densities we must employ transistors that have small geometries, typically \((4\mu m \times 4\mu m)\). Small geometries and subthreshold operation makes the drain current strongly dependent on variations of fabrication process parameters and in particular of the subthreshold intercept current \(I_0\) [Pa91].

Having addressed the energy dissipation/area efficiency problem at its root, we are left with problems of different kind i.e. (a) that of dealing effectively with transistor mismatch and (b) addressing defect and fault tolerance issues. Both are directly related to the underlying manufacturing technologies and will impose constraints on our design.
methodologies and organization of the systems. It is also safe to assume that future will not bring a perfect manufacturing technology, and that mismatch in devices as well as faults and failures are natural and they have to be addressed at the early stages of system integration.

Carver Mead points out that adaptation is a means of dealing effectively with individual component mismatch and failures [Me60]. We have argued towards a methodology that employs current-mode techniques with designs at the transistor level and minimal complexity circuits [An89, An90, An91]. Furthermore, we have demonstrated that there exist robust computational primitives such as distributed signal aggregation/normalization that can yield systems which degrade gracefully in the presence of localized faults [AnKo90].

There is no widely accepted definition for the current-mode approach in circuit design [CT90]. By current-mode, we shall refer to circuits that use both currents and voltages (like every electronic circuit) but where signals are represented as currents and voltages play only an incidental role. Translinear circuits in subthreshold MOS and BiCMOS [An89, An91] technologies are the classical example of a current-mode design technique.

Space does not permit a full discussion of issues involved. In the remainder of this short paper we will use examples of how design consideration at all levels and in particular how current-mode techniques have the potential for practical large scale analog computational systems.

2 Signal representation

One of the reasons that analog computational systems have a potential for higher computational throughput, is their effective use of interconnects. Long lines can be employed to aggregate signals if these are represented as currents. Current injectors are active devices; depending on the application, they operate above or below threshold. High bandwidth is achieved by keeping the voltage swings on these global lines as small as possible. In an actual implementation there is the choice of either bidirectional [Bo89a] or unidirectional signal [Bo89b] representations. Both approaches have advantages and disadvantages. In the first approach, currents can take both positive and negative values since they are supplied by devices of both polarity p-MOS and n-MOS. One physical line is thus adequate for encoding both positive and negative value signals. However, it has been our experience [Bo89a], that systematic transistor mismatch between devices of different types are deleterious and are problematic.

The alternative, which uses an extra line, employs unidirectional current signals. The current injecting devices are all of the same type and this overcomes the problem of systematic mismatch between n-type and p-type devices.

From a defect tolerance point of view, the differential encoding scheme is preferable. Usually, extra circuitry in the form of a mirror is used to invert and sum currents on a single line. This mirror introduces additional and perhaps unnecessary complexity and increases the possibilities for catastrophic defects and faults. That is why aggregation circuits employing the transconductance amplifier, which is a versatile functional block, should be avoided whenever possible and replaced by differential summing circuits.
3 Precision in computation

One of the challenges in the field of analog VLSI is the development of methodology that can yield working systems, despite the limited precision of the individual components. Based on extensive studies of production qualified processes [Pa91] from different manufacturers, it can be concluded that present day manufacturing technologies offer devices with threshold matching of as low as 0.5 mV. This is a very impressive number, and is based on analysis of random mismatch in measurements of over 150,000 transistors in large arrays. Random variations of device parameters are not deleterious in system performance when large number of devices contribute to the actual computation [An91]. However, hierarchical organization and sub-sections of increased precision may be necessary.

As an example, let us consider a Hamming distance classifier. At the highest level of organization, unary representation (as opposed to distributed) can yield systems with good storage capacity of one bit per stored for each bit of information [Bo89a]. Information is stored in binary form and fault tolerance can be attained by storing each vector in more than one location. Distributed representation could result in a system which may be more robust but not too useful in practice.

The organization of a Hamming distance classifier with unary representation involves a storage array, aggregating lines, and a functional block that performs the MAX computation [Bo89a, Bo89b]. This functional block, is often referred to as Winner Takes All (WTA) (Fig. 10 in [An91]). In the WTA cell itself, the current to voltage converting devices $M_1$ need to be accurate and thus can be replaced with bipolar transistors or large geometry MOS structures. The sizing of the devices depends on the actual size of the system (number of "neurons") and involves other factors such as the physical layout and compensation for the system dynamics. Note how such a simple realization of a circuit using minimal number of devices performs such difficult computation, finding the largest of a set of numbers.

4 Vision computation

An even more impressive high level function is attained by the current-mode implementation of a retina system for vision computation [An91, BoAn91].

Computation by "silicon retinas" exploits the aggregation properties of a resistive network which offer a very powerful computational primitive. However, an actual implementation of such systems requires active resistors as well as additional circuitry to compute differences in floating potentials. UV adaptation at the receptor level is also employed to compensate for individual transistor mismatch [Me90]. Since optical signals were compressed logarithmically and converted into voltages, their dynamic range is dramatically reduced. This introduces additional problems which can not be solved effectively by UV adaptation.

We have adopted a completely different design style [An91, BoAn91] that employs current-mode techniques and exploit the translinear properties of the MOS transistor; the computation is performed not in the voltage domain but rather in the current-domain. Taking differences of signals in space, is an essential operation for mapping elliptic partial differential equations on silicon. To do this we exploit common-substrate bias configuration of the subthreshold device physics. Thus diffusive networks can be implemented where signals now are represented as currents. The subthreshold transistor, operated in
this mode is termed a **difusor** (in analogy to a resistor). It can be shown that our system implements the optimum filter for regularized edge detection [Po85] with all variables represented as currents.

The system has been integrated in a 2 micron double poly double metal process. Out of the 24 chips tested all but one function as expected. In one of the chips, there is a blob of material that locally affects the operation. However, the remainder of the system functions properly. The chip has about 200,000 transistors all operating in subthreshold. Typical bias currents are a few nano-amperes. Since the system is sensitive to contrast, it is able to extract edges in low contrast scenes such as the outline of a yellow flower on a white background.

Currently, we are investigating the effects of actual layout defects in the performance of such systems. Results of our investigation will be reported in the future.

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**References:**


