Message from the Symposium Chairpersons

We would like to welcome you to the 2001 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems held in San Francisco! This is the first true year of the new millennium, and it marks the 16th in this long series of technical meetings, which began in 1986. It started with the IEEE Design for Yield Workshop, held in Oxford, UK in 1986. Then came the very successful series of the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems. With its ever-growing attendance this series was upgraded in 1996 to a Symposium. The changes are a mere reflection of the rapidly growing dependency of the society on the VLSI systems. In this 16th meeting, we vow to continue the tradition of bringing together academic and industry in the fields of defect and fault tolerance in VLSI systems and continue to be at the forefront of technical advancement.

This year our technical program has significantly expanded by 25%, with 14 single-track sessions with 56 accepted contributed papers covering a wide range of current issues in defect and fault tolerance in VLSI systems. The papers in the 14 regular sessions cover yield analysis, modeling and enhancement, fault-tolerance interconnections and systems, reconfiguration and repair, error coding, online testing, testing and BIST techniques, and fault injection techniques and environment. A special session on “Wafer Scale/Large Area Systems” is organized by one of the program co-chairs, Glenn Chapman, for the second year, to bring forth the latest progress in the VLSI systems to our participants. The authors came from all over the world: USA, Japan, Italy, China, Taiwan, India, New Zealand, Italy, France, Germany, Spain, Austria, Netherlands, Poland, Sweden, Belarus, Estonia and Canada; 14 countries in all. We are particularly pleased to find that many collaborations included in this year’s symposium were originated from the discussions at this Symposium previously.

We would like to thank the authors for their excellent contributions, the program committee and the external reviewers for their timely reviews and constructive feedbacks on the papers.

We hope you will find this Symposium to be technologically informative and stimulating. The exquisite location, in San Francisco, the gateway to Silicon Valley, will definitely help encourage many insightful discussions. Welcome old friends and new.

General Chairs

Susumu Horiguchi
Jien-Chung Lo

Program Chairs

Glenn Chapman
Regis Leveugle