Table of Contents

1998 International Symposium on Defect and Fault Tolerance in VLSI Systems

Message from the Symposium Committee ix
Acknowledgments xi

Keynote Address
Dealing with Defects in Very Deep Submicron Chips and Beyond
Yervant Zorian, LogicVision

Session 1: Yield and Defect Density
Chair: C. Drum, Lucent Technologies
1.1 Binning for IC Quality: Experimental Studies on the SEMATECH Data 4
A.D. Singh, D.R. Lakin II, G. Sinha, and P. Nigh
1.2 A Yield Improvement Program Using Process Control and Process Optimization for Particle Reduction Using In Situ Particle Monitoring on a Semitool Magnum 11
L.J.P. Vogels, M.W.C. Dohmen, P. van Duijvenboden, R.A. Latimer, and J.D.O. Heffernan
1.3 Management of Critical Areas and Defectivity Data for Yield Trend Modeling 17
S. Barberan and F. Duvivier

Session 2: Layout and Critical Area
Chair: V. Chiluvuri, Motorola
2.1 Yield and Routing Objectives in Floorplanning 28
I. Koren and Z. Koren
2.2 Orphan Metal Removal as an Element of DFM 37
N. Harrison
2.3 A Comparison of Efficient Dot Throwing and Shape Shifting Extra Material Critical Area Estimation 44
G.A. Allan

Invited Presentation
Hardware Fault-Tolerance Requirements for Very Deep Submicron
M. Nicolaidis, TIMA

Session 3: Reliability Enhancement
Chair: I. Koren, University of Massachusetts
3.1 A Fast Minimum Layout Perturbation Algorithm for Electromigration Reliability Enhancement 56
Z. Chen and F.-L. Heng
3.2 FPGA Design for Decimeter Scale Integration (DMSI) ..................................................... 64
   G.H. Chapman
3.3 Process Variations and their Impact on Circuit Operation ................................................. 73
   S. Natarajan, M.A. Breuer, and S.K. Gupta

Session 4: Defect and Fault Analysis

Chair: R. Mercer, A&M University
4.1 Comprehensive Defect Analysis and Defect Coverage of CMOS Circuits ......................... 84
   D. Al-Khalili, S. Adham, C. Rozon, M. Hossain, and D. Racz
4.2 Characterization of CMOS Defects Using Transient Signal Analysis ................................ 93
   J.F. Plusquellec, D.M. Chiarulli, and S.P. Levitan
4.3 Accurate Fault Modeling and Fault Simulation of Resistive Bridges ............................... 102
   V. Sar-Dessai and D.M.H. Walker
4.4 Functional Verification Coverage vs. Physical Stuck-at Fault Coverage ....................... 108
   X. Sun and C. Hull
4.5 An Integrated HW and SW Fault Injection Environment for Real-Time Systems .............. 117
   A. Benso, M. Rebaudengo, M. Sonza Reorda, and P.L. Civera

Panel Session: Fault Tolerance: Needs and Perspectives

Co-Organized with IEEE Design & Test of Computers
Moderator: J. Abraham, University of Texas at Austin
Panelists: B. Kaminska, Opmaxx Inc.
            R. Karri, Polytechnic University, New York
            H. Levendel, Motorola
            F. Lombardi, Northeastern University, Boston
            A. Nordsieck, The Boeing Company

Session 5: Testing Techniques

Chair: V. Piuri, Politecnico di Milan
5.1 Increasing Current Testing Resolution ............................................................................. 126
   C. Thibeault
5.2 On-Chip Test Embedding for Multi-Weighted Random LFSRs ..................................... 135
   D. Kagaris, S. Tragoudas, and A. Majumdar

Session 6: Testing of Regular Structures

Chair: T.M. Mak, Intel Corporation
6.1 A New Method for Testing EEPLA’s .................................................................................. 146
   A. Munshi, F.J. Meyer, and F. Lombardi
6.2 C-Testable One-Dimensional ILAs with Respect to Path Delay Faults:
   Theory and Applications ............................................................................................... 155
   T. Haniotakis, Y. Tsiatouhas, and D. Nikolos
6.3 On the Complexity of Sequential Testing in Configurable FPGAs .......... 164
W. Feng, W.K. Huang, P.J. Meyer, and F. Lombardi

**Session 7: Concurrent Testing Techniques**

**Chair:** P. Lala, University of South Florida

7.1 Signal Coding Technique and CMOS Gates for Strongly Fault-Secure Combinational Functional Blocks ......................... 174
C. Metra, M. Favalli, and B. Ricco

7.2 Systematic AUED Codes for Self-Checking Architectures .................. 183
D. Sciuto, C. Silvano, and R. Stefanelli

7.3 Challenges of Built-In Current Sensor Designs .......................... 192
Y.-Y. Guo and J.-C. Lo

**Session 8: Fault Diagnosis**

**Chair:** A. Singh, Auburn University

8.1 On the Current Behavior of Faulty and Fault-Free ICs and the Impact on Diagnosis .............................................................. 202
C. Thibeault and L. Boisvert

8.2 A Systematic Approach for Diagnosing Multiple Delay Faults ............. 211
J.G. Dastidar and N.A. Touba

8.3 Diagnosis of Scan Chain Failures ........................................ 217
Y. Wu

**Session 9: Fault-Tolerant Designs I**

**Chair:** E. Fujisawa, Tokyo Institute of Technology

9.1 Error-Correcting Goldschmidt Dividers Using Time Shared TMR ............. 224
W.L. Gallagher and E.E. Swartzlander Jr.

9.2 Fault-Tolerant Voting Mechanism and Recovery Scheme for TMR FPGA-Based Systems .................................................. 233
S. D’Angelo, C. Metra, S. Pastore, A. Pogutz, and G.R. Sechi

9.3 Reducing Fault Sensitivity of Microprocessor-Based Systems by Modifying Workload Structure ........................................ 241
D. Audet, S. Masson, and Y. Savaria

**Session 10: Fault-Tolerant Designs II**

**Chair:** T. Nanya, University of Tokyo

10.1 Transient and Intermittent Fault Recovery without Rollback .............. 252
S.N. Hamilton and A. Orailoglu

10.2 Highly Reliable Systems with Differential Built-In Current Sensors ....... 261
J.-C. Lo

10.3 A Silicon Compiler for Fault-Tolerant ROMs ................................ 270
A. Gupta, K. Chakraborty, and P. Mazumder

10.4 Self-Reconfiguration Scheme of 3D-Mesh Arrays .......................... 276
S. Horiguchi and I. Numata
**Session 11: High-Level Synthesis of Reliable Systems**

*Chair: J.C. Le, University of Rhode Island*

11.1 A System for Evaluating On-Line Testability at the RT-Level ........................................ 284  
   S. Chiusano, F. Corno, M. Sonza Reorda,  
   and R. Vietti

11.2 High-Level Synthesis of Data Paths with Concurrent Error Detection ............................ 292  
   A. Antola, V. Piuri, and M. Sami

11.3 Graceful Degradation in Synthesis of VLSI ICs ............................................................. 301  
   A. Orailoglu

11.4 Designing for Yield: A Defect-Tolerant Approach to High-Level Synthesis ................. 312  
   M. Broglia, G. Buonanno, M.G. Sami,  
   and M. Selvini

11.5 High-Level BIST Synthesis for Delay Testing ............................................................... 318  
   X. Li and P.Y.S. Cheung

**Session 12: Yield and Reliability Issues of Analog and Mixed Signal Circuits**

*Chair: D. Goodman, Opmaxx Inc.*

12.1 Yield Enhancement by Multi-Level Linear Modeling of Non-Idealities  
   in an Interpolated Flash ADC ......................................................................................... 326  
   A. Boni and A. Pierazzi

12.2 Specification-Driven Test Design for Analog Circuits ............................................... 335  
   P.N. Vartiyam and A. Chatterjee

12.3 Modular Fault Simulation of Mixed Signal Circuits with Fault Ranking  
   by Severity ......................................................................................................................... 341  
   A.V. Gomes, R. Voorakaranam, and A. Chatterjee

12.4 BIST Module for Mixed-Signal Circuits ........................................................................ 349  
   S. Demidenko, V. Piuri, V. Yarmolik,  
   and A. Shmidman

**Author Index** ................................................................................................................. 355