Three-dimensional stacked ICs hold the promise of heterogeneous integration, inter-die connections with increased performance at lower power dissipation, and increased yield and hence decreased product cost. However, all of the above can only become true if 3D-SICs can be properly tested for manufacturing defects. Companies have started to develop their test strategies for these products, and the outcome is largely dependent on (1) the necessity of test generation for specific new 3D defects, (2) the feasibility of access the test targets, and (3) the economic trade-offs involved. Test research is needed to create options for these challenges.