Foreword to the 12th IEEE DDECS Symposium

The DDECS Symposium, until 2008 Workshops, has been organized annually in Czech Republic (1995, 2002, 2006), Poland (1997, 2003, 2007), Slovakia (2000, 2004, 2008) and Hungary (2001, 2005). It offers a forum for exchanging ideas, presenting research results as well as practical applications in the fields of design, verification, test and diagnosis of electronic circuits and systems. Over the years, DDECS has earned a high world-wide reputation. This year, the DDECS symposium takes place in Liberec, Czech Republic, and is organized by the Technical University of Liberec. It will host many researchers, PhD students and experts from universities and the industry. The symposium is sponsored by the IEEE Computer Society, the Test Technology Technical Council and despite the economical crisis also by the following industrial partners: Nadace Preciosa, H test, ASICentrum and CUBE CZ.

This year, 91 papers were submitted from 26 countries in Europe, Asia, and America. Thanks to the precious work of the Programme Committee members and based on more than 250 reviews, a high-quality technical program for the three-day symposium has been set up. The technical program consists of three keynote speeches about problems and innovations concerning the design and test of electronic circuits and systems implemented by emerging technologies. There will be eight regular, one industrial, two student and three poster sessions gathering 33 oral presentations and 25 posters.

A commission established from DDECS Steering Committee members and the DDECS 2008 workshop chairs selected two best papers presented at DDECS 2008 – one from the design field and the other from the test field. The commission took into consideration the papers' ranking based on the review process, the quality of their publication in the proceedings, and the authors' oral presentations. The prize for the best papers at DDECS 2008 has been conferred to the following papers:

Tomasz Borejko and Witold A. Pleskacz, A Resistorless Voltage Reference Source for 90 nm CMOS Technology with Low Sensitivity to Process and Temperature Variations, Warsaw University of Technology, Poland (design field)

Andrzej Krasniewski, Concurrent Error Detection for Combinational Logic Blocks Implemented with Embedded Memory Blocks of FPGAs, Warsaw University of Technology, Poland (test field).

The DDECS Steering Committee is grateful for the effort and the excellent voluntary work of many individuals and organizations, in particular, the members of the Programme Committee and the Organization Committee, as well as the Technical University of Liberec, the IEEE Computer Society, and the Test Technology Technical Council for preparing DDECS 2009 and mayor of the town Liberec for his auspices of the event.

We wish all symposium participants interesting presentations and an opportunity to refresh contacts and set-up new ones and to find ideas for future cooperation. Furthermore, we wish all visitors a pleasant and inspiring atmosphere during the IEEE DDECS 2009 Symposium in Liberec.

Welcome to the IEEE DDECS Symposium in Liberec!

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