Proceedings
2005 IEEE International Workshop on
Current & Defect Based Testing (DBT 2005)

IEEE International Workshop on
Current & Defect Based Testing

Palm Springs, CA

May 1, 2005
Lodge at Rancho Mirage, Palm Springs, USA

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Sponsored by:
IEEE Computer Society Test Technology Technical Council
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(DBT-2005)

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Coordinator: Hank Walker, Texas A&M University, USA
Message from the General Chairs and Program Chair

It is our pleasure to welcome you to the 2005 IEEE International Workshop on Current and Defect Based Testing (DBT2005). The DBT2005 workshop is being held in conjunction with the VLSI Test Symposium (VTS2005), in Palm Springs, CA. The theme of this year’s workshop “Realizing Defect-Based Test in Production Test Flows” has been selected to generate active discussion on the challenges that must be met to ensure high IC product quality through to the end of the decade.

One of the fundamental questions in the testing community is the effectiveness of defect-based testing approaches in the production test flow. Defect-based testing has the potential to better handle emerging defect types and changing circuit sensitivities in VDSM circuits compared to conventional stuck-at (structural) test.

The IEEE International Workshop on Current and Defect Based Testing (DBT 2005) is aimed at addressing these issues and other issues related to “Realizing Defect-Based Test in Production Test Flows”. Paper presentations on topics related to those given below are expected to generate active discussion on the challenges that must be met to ensure high IC quality through the end of the decade.

The keynote, papers and panel topic selected for this workshop address these needs. Chuck Hawkins from University of New Mexico will open up discussions with his presentation entitled “We Are at the Next Test Paradigm & Other Topics”. The technical program that follows consists of selected presentations on important defect-based methods and their applications including IDDX applications & monitor design 1 & 2, defect data analysis, innovative defect-based test approaches, followed by an afternoon Keynote titled “Defect Trends – Yesterday, Today and Tomorrow” by Anne Gattiker from IBM. A panel rounds out the day to discuss issues related to the topic “Defect Based Testing in a Foundry Environment: Holy Grail or Reality?”

This workshop is the result of considerable time and effort from many dedicated individuals in the field. We wish to thank the authors for submitting their work and the many reviewers for their timely reviews. We are thankful to the Program Committee and the Steering Committee for ensuring a quality program and with the organization of the workshop. We gratefully acknowledge the continuing support of the IEEE Computer Society Test Technology Technical Council.

We hope you will find the workshop to be thought provoking and informative.

Welcome to DBT2005!

Sankaran Menon Hans Manhaeve Jim Plusquellic Mehdi Tahoori
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Keynote Address - 1:

“We Are at the Next Test Paradigm & Other Topics”

Chuck Hawkins, University of New Mexico, USA
DBT-2005 Keynote Address - 1:

“We Are at the Next Test Paradigm & Other Topics”

by:

Chuck Hawkins,
University of New Mexico, USA

ABSTRACT

Our major test practices came out of the 1950s and evolved from functional testing, to fault model testing, to defect-based testing, and now we have entered another. It may be time to recognize this and fold it into our paradigms. This talk will discuss the IC world we're in now and will enter and a look at the options. A breakthrough technique in rapid location of defective vias is described and used to complement the description of difficult “Nanometer” failure mechanisms.

Chuck Hawkins is a Professor in the Electrical and Computer Engineering Department at the University of New Mexico. He teaches graduate courses in Microelectronics Design, Reliability, Test Engineering, and Failure Analysis. He has also taught industry short courses on these topics in the USA, Canada, Europe, and Australia for over twenty years. His research in these topics includes a twenty year research collaboration with the Microelectronics Group at Sandia National Laboratories in Albuquerque, New Mexico USA, a four year collaboration with the AMD Corporation and Sandia Labs in failure analysis of timing paths in high speed microprocessors, and a four month sabbatical with Intel Corporation in Rio Rancho, New Mexico USA.

He was the Editor of the ASM Electron Device Failure Analysis Magazine (EDFA) from 1999 – 2003, and serves on the EDFAS Board of Directors. He was the General and Program Chair of the International Test Conference (ITC) in 1996 and 1993 respectively. He co-shared eight Best or Outstanding Paper conference awards with colleagues at Sandia Labs, Intel, and AMD Corp at ITC, and at the International Symposium on Test & Failure Analysis (ISTFA). He has co-authored three books on Electronics, including the recent CMOS Electronics: How it Works, How it Fails by Wiley-IEEE Press in 2004. He received his Ph.D. from the University of Michigan in Bioengineering, a Masters in Electrical Engineering from Northeastern University, and a BEE from the University of Florida. He was the Associate Dean of the School of Engineering at the University of New Mexico in 1980-82. He has held summer faculty appointments at the University of the Balearic Islands in Spain from 1998 – 2002.
Keynote Address - 2:

“Defects Yesterday, Today and Tomorrow: Implications for Test”

Anne Gattiker, IBM Austin Research Laboratory, USA
ABSTRACT

This talk proposes a context for discussing sources of IC failure and presents a round-up of evidence for characteristics of defect affecting past and current technologies. It discusses trends for future technologies, including systematic defects and unacceptable process variations, and their implications for test.

Anne Gattiker is a Research Staff Member at IBM. She began her career in IBM’s Worldwide Test Engineering group in Burlington, VT and now works at the IBM Austin Research Lab in Austin, TX. She is an ITC best paper award winner and is the Technical Program Vice Chair for ITC 2005. She holds a Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon University.