**TUTORIALS**

**B  Electronic Systems and Interfaces for Innovation in Life Sciences and Biomedical Applications**

Organisers: Georges Gielen, KU Leuven, BE  
Carlotta Giuducci, EPFL Lausanne, CH

Speakers: Carlotta Giuducci, EPFL Lausanne, CH  
Roland Thewes, TU Berlin, DE  
Wolfgang Eberle, IMEC, BE  
Marco Bianchessi, STMicroelectronics, IT

The interface between electronic circuits and life sciences is one of the focal points of future integrated system design. Applications include biomolecule detection, biosensor arrays, deep brain stimulation, cardiac cell monitoring, among many others. Several solutions for electronic devices/biological matter interactions are already available and they have proven their potential to be highly-portable systems or high-throughput systems or both. In this tutorial, we will address in detail the challenges in design and implementation of electronic sensors, circuits and systems as privileged means to interact with biological matter while bringing the advantage of almost unlimited choice of signal processing, storing and communication solutions. All aspects will be covered, ranging from providing an overview of different sensing solutions, discussing the architectural and circuit design issues to illustrating the packaging and testing solutions for both in vitro and in vivo applications. The tutorial scope goes from advanced research to commercial applications that are available on the market.

**C  State-of-the-Art and Challenges in ESL-Verification**

Organiser: Volkan Esen, Infineon Technologies AG, DE

Speakers: Oliver Bringmann, Forschungszentrum Informatik FZI, DE  
Wolfgang Ecker, Infineon Technologies AG, DE  
Erhard Fehlauer, Fraunhofer IIS/EAS Dresden, DE  
Daniel Grosse, Bremen U, DE  
Christoph Kuznik, Paderborn U, DE  
Jan-Hendrik Oetjens, Robert Bosch GmbH, DE  
Andreas v. Schwerin, Siemens AG, DE

The increasing complexity of embedded systems has driven the development of new abstract modeling techniques, leading to the so-called Electronic System Level (ESL). For ESL design SystemC has become the de-facto system description language. In SystemC the most popular and widely used abstraction level is Transaction Level Modelling (TLM). Over the last years intensive research in academia and industry brought new methodologies and modelling standards such as OSCI TLM2 to today’s virtual prototype development. Virtual prototypes are used for many different tasks, as e.g. early SW development. As SW development based on virtual platforms is possible long before the silicon is available, the design productivity increases significantly.

However, to fully benefit from the productivity gain possible, the bottleneck of functional verification has to be addressed. Therefore, in the recent years different methodologies and approaches have been developed which target the verification of TLM designs and virtual prototypes. This tutorial outlines the verification challenges for SystemC models and in particular for ESL. Furthermore, different verification tasks are considered and the respective verification approaches are explained. It is shown to what level verification of TLM-models can be done with today’s verification methodologies and pros and cons of the approaches are discussed.

**D  Chip-Package Co-Design Challenges for 3D Integration**

Organisers: Herb Reiter, EDA2ASIC, US  
Pol Marchal, IMEC, BE

Speakers: Jochen Reisinger, Infineon, DE  
Geert van der Plas, IMEC, BE  
Ravi Varadarajan, Atrenta  
Ghislain Kaiser, Docea Power  
Edmund Cheng, Gradient DA  
Dragomir Milojvic, IMEC, BE  
Peter Schneider, Fraunhofer IIS/EAS Dresden, DE  
Terry Ma, VP TCAD, Synopsys  
Vassilios Gerousis, Cadence  
Yann Guillou, STE  
Jean Christophe Eloy, Yole

This tutorial will review new 3D integration technologies and their impact on chip-package co-design.
In the morning, the tutorial will highlight the continuing needs for higher levels of integration and the mandates imposed by the stringent cost- and power constraints. The presenters will address the many benefits but also challenges 3D chip-stacking introduces and suggest methods to adopt the design of dies and advanced packages to higher levels of integration. In addition to new EDA tools and flows, our industry is adopting a new design practice: physical design prototyping of chip stacks. Several experts from industry and academia will share their experience and offer advice before the lunch break.

In the early afternoon session a representative from academia and two major EDA vendors will talk about the multi-physics challenges that need to be considered, both in new EDA flows and the physical design prototyping, to assure success.

Finally, two talks providing an outlook of how 3D technologies impact current and future products will summarise and end the day.

A1 AUTOSAR
Organiser: Simon Fuerst, BMW Group, DE
Speakers: Simon Fuerst, BMW Group, DE
Gerulf Kinkelin, PSA, FR

The objective of the tutorial is to give an overview on the following main topics:

- Motivation and principles of AUTOSAR
- The technological conception of AUTOSAR
- The development of the AUTOSAR standard

AUTOSAR has been founded as a development partnership in 2003. The common vision was to pave the way for innovative electronic systems by establishing an open industry standard for the automotive software architecture between suppliers and manufacturers. The core partners and more than 170 members produced the first set of major specifications end of Phase I in 2006, meanwhile the standard is already being exploited by all major OEMs and 1st Tiers. The development of the cooperation and the roll-out of a standard will be explained.

The technical scope of AUTOSAR focuses on three main working topics: Basic Software Architecture, Methodology and Templates, and Application Interfaces. Thereby AUTOSAR consolidates existing design elements and new concepts into a coherent standard. The tutorial will show how the organisation of AUTOSAR has been adapting to the ever changing challenges of the automotive market. Currently about 25 work packages are working on developing the specifications.

Though Phase I and II releases R1.0/R2.0/R2.1/R3.0/R3.1 have been made available, while R4.0 followed end of 2009. Details on all major achievements of AUTOSAR Release 4.0 will be presented. In the beginning of 2010 AUTOSAR Phase III has started and will last till end of 2012. The planning of this phase will be presented and details on the new concepts will be given that will extend the AUTOSAR standard will be given.

E1 IC Yield, Reliability and Prognostic Methods using Nanoscale Test Structures
Organisers: Yiorgos Makris, Yale U, US
Dimitris Gizopoulos, Piraeus, U, GR
Speakers: Hans Manhaeve, Qstar Test, BE
Douglas Goodman, Ridgetop Group

The mounting issues of decreased yield and reliability from nanoscale IC processes require advanced approaches to the measurement and mitigation of device degradation and variance. Shrinking process geometries, with their corresponding reduction in device lifetimes, have broad implications to critical applications having long intended design lifetimes. Nanoscale transistor sizes are emerging as a major concern to the long term reliability of safety-critical systems in aerospace and automotive applications. Common semiconductor failure modes include Time Dependent Dielectric Breakdown (TDDB), hot carrier damage (HCl), and Negative Bias Temperature Instability (NBTI). Die-level prognostic test structures can detect and help mitigate the untimely failures in critical systems. These test structures, with variance measurement capabilities, also provide an effective platform for improved process-aware design for improved yields. This tutorial will address concepts of in-situ test structures as a solution to yield, reliability and prognostic applications and include practical application examples.

This tutorial is part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP)

F1 Application of the SystemC AMS Standard
Organiser: Martin Barnasconi, NXP Semiconductors, NL
Today's embedded systems interact more tightly with the analog physical environment, where digital HW/SW subsystems becomes functionally interwoven with analogue/mixed-signal (AMS) blocks such as RF interfaces, power electronics, or sensors and actuators. Examples are cognitive radios, sensor networks or systems for image sensing. This requires new means to model and simulate the interaction between AMS subsystems and HW/SW subsystems at functional and architecture level. Especially for this purpose, the SystemC language standard has been extended with AMS capabilities. This tutorial will present the motivation and unique capacities of the SystemC AMS extensions for industrial applications in wireless communication and automotive. New modelling concepts and design refinement methods for mixed-signal systems are explained. An application example of a heterogeneous wireless sensor network is presented, covering modelling across several disciplines (physics, digital, analogue/RF, software), modelling principles and numerical analysis methods.

This tutorial targets hardware and system engineers, architects and verification engineers active in industrial projects where analogue and digital functionality comes together. The tutorial will bring hands-on experience how to efficiently use the SystemC AMS extensions for system design and verification tasks.

**A2 Asynchronous Logic and GALS Design: Principles and State-of-the-Art**

Organisers: Pascal Vivet, CEA-LETI, FR  
Alex Yakovlev, Newcastle U, UK

Speakers: Alex Yakovlev, Newcastle U, UK  
Jens Sparso, TU Denmark, DK  
Yvain Thonnart, CEA-LETI, FR  
Pascal Vivet, CEA-LETI, FR

The growing variability and complexity of advanced CMOS technologies makes the physical design of clocked logic in large Systems-on-Chip (SoC) more and more challenging. Asynchronous logic has been studied for many years and become an attractive solution for a broad range of applications, from massively parallel multi-media systems to systems with ultra-low power consumption, energy autonomous systems, and sensor-network nodes.

The objective of this tutorial is to give a comprehensive overview of asynchronous logic. The tutorial covers the basic principles and advantages of asynchronous logic, as well as deeper insights such as high level modelling, synthesis methods, architecture issues such as arbitration or de-synchronisation techniques. The tutorial also presents the Globally Asynchronous and Locally Synchronous (GALS) design style as an intermediate design solution which is particularly adapted to Network-on-Chip (NoC) architectures. The tutorial finally provides an overview of state-of-the-art circuits and start-up companies.

This tutorial targets VLSI design engineers, technical managers, researchers and students working in the area of SoC design and all those who would like to know more about these technologies that are becoming more and more mature.

**E2 Testing Low-Power Integrated Circuits: Challenges, Solutions, and Industry Practices**

Organisers: Yiorgos Makris, Yale U, US  
Dimitris Gizopoulos, Piraeus U, GR

Speakers: Srivaths Ravi, Texas Instruments, US  
Mohammad Tehranipoor, Connecticut U, US  
Rohit Kapur, Synopsys, US

The push for portable, battery-operated, and “cool-and-green” electronics has elevated power consumption as the defining metric of integrated circuit (IC) design. Testing ICs built for such applications requires judicious consideration of test power implications on various aspects of the design cycle (e.g., packaging and power grid design), test engineering (multi-site ATE power supply limitations and board design), power-aware test planning (DFT and ATPG), and developing the enabling EDA tool infrastructure (SW for estimation, reduction and low-power test generation). Furthermore, with power optimisation and management techniques becoming “de-facto” in almost all emerging 45nm and lower chips, systematic testing of these structures and the device in the presence of these structures becomes mandatory. This tutorial is intended to provide an in-depth and up-to-date understanding of low-power IC testing covering (a) dimensions of power-aware testing, (b) techniques for estimation and reduction of test power consumption and (c) test of power managed designs. Case-studies illustrating industrial design deployment practices and existing EDA vendor support will be outlined to illustrate capabilities and gaps in the state-of-the-art.
In order to improve verification productivity, engineers are faced with a classic choice: work harder or work smarter. Working harder means either putting in more hours or determining how to apply the same verification techniques you’ve been using to larger and more complex designs without going insane. Working smarter, on the other hand, involves adopting new techniques and advanced technologies that complement what you’re used to doing, but rely on tools and automation to accomplish the necessary efficiencies.

This tutorial will demonstrate an advanced verification flow, showing how the latest verification technologies can be combined within an efficient methodology to provide a highly effective and productive verification of an SoC design. Beginning with a discussion of verification requirements, we will show how to create a verification plan that involves requirements beyond just random constraints and coverage, and to build a comprehensive verification environment to meet those requirements.