Are we there yet?
Has IP block assembly become as easy as LEGO?
Where are we going? Are HW/SW Subsystems the future of IP?

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Abstract — With the majority of chip real estate being filled with re-used IP blocks, the process of block assembly has significantly grown in importance. Marketing literature seems to suggest that assembling a chip from IP is as easy as browsing a library of blocks, assembling them in a block diagram and then pushing a button.

Are we there yet? Is it like the assembly of LEGO blocks? In parallel, the evolution of IP-reuse has gone through various stages from smaller blocks like multipliers and adders to more complex blocks like USB, SATA, PCI and others. What is the next step up from here? Given the growing importance of software, a new form of re-use has started to emerge, that is re-use at the sub-system level, often including hardware and software.

This panel will explore the trends in IP re-use and discuss where IP blocks end and systems start. Furthermore, it will also explore the trends in IP-reuse and assembly, assess the state of the art of IP assembly and co-simulation standards like IP-XACT and OSCI TLM-2.0.

Starting from IP assembly approaches at the RT-level, the panel will chart the direction where IP assembly will go from here towards re-use and assembly at the transaction level.

IP-Reuse, HW/SW Subsystems, IP Assembly