Session 38
Panel: Deep Submicron Design Challenges

Chair: Mike Smith - Compass Design Automation, San Jose, CA
Organizers: Bob Wiederhold - High Level Design Systems, Santa Clara, CA
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This panel will provide access to a group of ASIC engineers familiar with the problems of deep
submicron design that will face us in the near future.

As we move to deep submicron CMOS processes we are scaling the metal linewidth but not the
thickness. This is increasing the parasitic capacitance of the wires to the point where the typical
interconnect delay is larger than a gate delay. At the moment synthesis tools work by minimizing the
number of literals in Boolean logic expressions and mapping to gates in a cell library with the smallest
databook delay values. Instead of concentrating on logic synthesis and pre-layout simulation and adding
the wires, almost as an afterthought, we will need to think far more carefully about interconnect. One of
the ways to do this is to couple the synthesis and physical layout steps far more tightly than they are now.
It is not at all clear how best to do this.

Interconnect is one of the biggest, most visible, and perhaps most easily understood problems in deep
submicron design, but there are others. In fact, there are many second- and third-order physical effects
that are starting to become more important. In the past we have swept these problems under the carpet by
using worst-case design. We can no longer afford the increasing number and increasing size of these
pessimistic assumptions.

Some other examples of effects we will need to consider:

We will have to pay more attention to the shape of logic waveforms and not just their delay. Many ASIC
vendors have already started to account for the effect of rise and fall times.

We will need to develop methods to tackle interconnect coupling. We cannot afford to extract all
coupling capacitances.

With deep submicron processes we are moving into an era where we need low-power design, since
batteries and packages don\'t seem to be keeping up. We need new tools and methods to help us in this
area.

Lithography is becoming very difficult as we run out of room in the light spectrum. At the moment we
put what we want on a mask and expect the lithography engineers to reproduce it on silicon. This may
not continue to be possible.

Panel Members:

David Gregory - Synopsys, Inc., Sunnyvale, CA
Jim Hogan - Cadence Design Systems, Inc., San Jose, CA
Tsutomu Iio - Toshiba Corp., Kawasaki, Japan
George Janac - High Level Design Systems, Santa Clara, CA
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Scott Nogueira - Sun Microsystems, Inc., Chelmsford, MA