Panel: Power Minimization in IC Design

Chair: Massoud Pedram - Univ. of Southern California, Los Angeles, CA  
Organizer: Robert Dahlberg - EPIC Design Technology Inc., Santa Clara, CA

Mobile and portable information systems are pushing electronics and the development process. In their wake are new requirements that drive low-power design. This is however by no means the only driving force behind the need for a dramatic reduction of power dissipation in digital ICs. There also exists a strong demand on producers of high end products to reduce power consumption. Power minimization is thus vital for different reasons in different applications.

Design knowledge and experience in minimizing power while optimizing performance is very limited. Low-power design is in its infancy. The same can be said for design tools. The opportunities for ultra low power tools and methodologies that achieve dramatic reduction of power and push higher up the design entry point are all around us. However, the need for tools that broaden the low-power design envelope is not being articulated by the user community very strongly.

This panel seeks to expose solutions that designers and EDA vendors have, to present proper vehicles for transferring the low power design techniques and methodologies to the user community, and to provide a forum for exploring what is still needed. What design paradigms make sense, what levels of accuracy and speed are acceptable to the users and what tools have the highest payoff are part of what this panel is all about.

Panel Members:

Walter Davis - Motorola, Boynton Beach, FL  
Adel Khouja - Synopsys, Inc., Mountain View, CA  
Uming Ko - Texas Instruments Inc., Dallas, TX  
Raymond Leung - LSI Logic, Milpitas, CA  
Simon Napper - EPIC Design Technology Inc., Santa Clara, CA  
Stefaan Note - Philips ITCL, Leuven, Belgium  
Jan Rabaey - Univ. of California, Berkeley, CA