IPDA: Interconnect Performance Design Assistant

Norman H. Chang, Keh-Jeng Chang, John Leo, Ken Lee, and Soo-Young Oh

Hewlett-Packard Company, Palo Alto, CA 94304

Abstract

IPDA is a generic interconnect performance design assistant that integrates a finite-difference numerical simulation method, linear interpolation algorithm, interactive performance synthesis methodology, and lossless/lossy transmission-line SPICE modeling capability into a spreadsheet-style graphical user interface. It assists in selecting interconnect technologies for design-for-performance goals and also in optimizing interconnect performance designs for the full hierarchy of packaging including IC/MCM/PCB/via interconnect designs. Although this paper describes electrical performance measures for given geometries and material parameters of conductors and dielectrics, IPDA can also be customized for other packaging measures such as reliability, thermal and cost effects through spreadsheet interface and calculations.

1 Introduction

Multi-level interconnect technologies (MLITs) have been widely used for on-chip and off-chip interconnections in VLSI/ULSI systems. Interconnect delays have constituted a large percentage of the total system delays. In high-frequency cases such as GaAs digital design, the interconnect delay is above 70% of the total delay [1]. However, we observe that MLIT modeling is still an ad-hoc process in the IC/packaging industry with very few CAD tools available to increase the productivity.

There are three major obstacles for efficient MLIT designs. First, the scaling of recent MLITs has made analytical and empirical formula obsolete [2,3]. 3-D structures such as dual signal stripline, via, lead attachment, and trace bends require 3-D numerical simulations for accurate impedance control, noise margin and delay simulation, and so on. However, the drawbacks of ad-hoc 2-D/3-D numerical simulations are time-consuming and tedious [4]. A solution is needed to provide MLIT designers accurate and immediate performance information.

Second, more and more high speed systems designs demand that engineers consider the full hierarchy of packaging designs. In particular, chip to chip communication through the hierarchy of packaging structures is crucial to system performance and cost. Figure 1 shows a typical view of such an interconnection [5]. A signal travels from an output driver pad to a receiver pad through a solder bump, short transmission line on the carrier, via through the carrier, solder bump to the substrate, transmission line on the substrate, and the same connection through the receiver carrier in the reverse order. An immediate question posed to the designer is what combination of technologies from the full hierarchy of packaging categories (i.e. IC processes, MCM/PCB/via/lead attachment technologies) will satisfy the system performance specification such as delay, and noise margin requirements. A common interconnect modeling methodology is therefore needed to integrate and optimize the design of disparate interconnect domains such as IC, MCM, PCB, via, and lead attachment. For long interconnects, lossless and/or lossy transmission line effects have to be considered for dramatic changes of interconnect pitches which greatly affect the trace resistance. Although MLIT performance simulation with non-linear driver/receiver characteristics is time-consuming, it has been indispensable for designers of high speed systems [6]. CAD tools have to be integrated to handle this easily and efficiently.

![Figure 1. Chip to chip signal communication through the full hierarchy of packaging elements.](image)

2 Overview of IPDA

IPDA integrates four subsystems: (1) a batch-mode computation that combines 2-D/3-D finite difference numerical simulations and a fast interpolation algorithm; (2) an interactive design of MLITs through performance browser, synthesis, and on-line evaluation panel; (3) an interactive SPICE subcircuit/circuit generations and simulation; and (4) a spreadsheet-style graphical user interface environment for customization. The functionalities of the four sub-
2.1 Batch Mode Computation

The batch mode computation algorithm is derived from the HIVE system of IPDA are described below.

The batch mode computation algorithm is derived from the HIVE algorithm [9], which computes selective lateral and vertical capacitances of sub-micron IC interconnect using an internally developed tool based on finite-difference methods [10]. The non-calculated capacitances can then be obtained through fast interpolation.

We decided to take advantage of HIVE after we found that the assumptions of extracting submicron on-chip interconnect capacitances reported in [9] are also valid for MCM and PCB. To be specific, first, interline ("CII") and vertical ("Cg") capacitances are linearly dependent on width when the interline spacing is fixed. Second, with enough points of numerical simulations on capacitances when interline spacing is varying and width fixed, other capacitances for any spacings bounded by the simulated spacings can be interpolated.

For example, Figure 2 illustrates that both the changes of "CII" and "Cg" for a thin-film MCM behave linearly when the width is changed but the spacing is fixed. Therefore, for a fixed spacing, we only need to calculate two capacitances using numerical simulation and are able to interpolate the capacitance values for different widths. However, due to slight neglect of non-linearity of capacitance curves vs. spacing when the width is fixed as shown in Figure 3, we need to take more points using numerical simulations and do a linear, polynomial, or cubic spline interpolations for different spacings depending on the accuracy wanted. In either way, the interpolated capacitances are carefully checked to have the maximal induced error to be around 3% of the capacitance.

IPDA enhances the HIVE's batch mode by automating the setup of batch mode computation for new constructions and extending the application to packaging domains. Each new MLIT construction is specified with a common set of characteristic parameters, such as number of layers, dielectric constants, dielectric thicknesses, conductor type, soldermask or overcoat dielectric constant and thickness, outer layer and inner layer conductor thicknesses, and number of coupling traces. Since different interconnect domains have different set of characteristic parameters, the current IPDA has three construction examples: MCM_1, MCM_2, and MCM_3.

![Figure 4. A construction worksheet for MCM thin film.](image)

Representative data points for interconnect capacitances are extracted numerically for all the conceivable models of a new construction in the batch mode. For example, a 4-layer MCM construction can be modeled with strip line (SL), dual stripline (DSS), surface microstrip (SM), and buried microstrip outer (BMO), etc. A linear interpolation algorithm can then be applied to generate any other points bounded by the width/spacing ranges of the simulated points. The simulated capacitances are subsequently used to derive inductances L and transmission line properties, including Zo, Zo', Zo (odd, even, effective mode impedances), Pd, Pd, Pd (odd, even, effective propagation delays) [11], and Vp, Vp (backward, forward crosstalks) [12,13] for all the interconnect models. Below we show the key equations for obtaining the performance parameters. First, C and C'(capacitance obtained by setting all E, = 1) matrices are obtained from simulation or interpolation.

\[
L = \left( \frac{C}{E_r} \right)^{-2} \left( \frac{C'}{E_r} \right)^{-1}
\]

where c is the speed of light, Er is the relative permeability of the dielectric, assuming TEM or quasi-TEM mode.

\[
Z_o = \frac{L_{11} + L_{12}}{C_{11} + C_{12}}
\]

\[
Z_o = \frac{L_{11} - L_{12}}{C_{11} - C_{12}}
\]
2.2 Interactive Mode

The cost-performance parameters to be considered in optimizing a high speed, fast delivery, and low cost RISC system include not only "conventional" design parameters (e.g. loaded gate delays, interconnect delays, EM interference, power dissipation, and clock skew) but also cost and material concerns (e.g. cost, yield, device technologies selection, MLIT technologies selection, MLIT pitch optimization, lead attachments selection, chip footprints, and packaging sizes). The interactive mode of IPDA represents our first step to assist designers making trade-off. It provides designers an on-line tool to help optimize multi-level interconnect design and/or to obtain appropriate geometries which can satisfy the desired performance goals. The following interactive functions are provided by IPDA: goal-directed interconnect synthesis, design optimization through X-Y graphing, and on-line evaluation. IPDA provides immediate results to the users and the average execution times of the three functions in an HP/Apollo 720 workstation are within 1 second while 2-D/3-D add-hoc simulations take about 20 to 1000 seconds. Therefore, the time for IPDA to calculate tens to hundreds of data points of all the user-specified models for a construction is much faster than 2-D/3-D add-hoc simulations which provide single data point for a specified geometry.

2.2.1 Goal-directed Interconnect Synthesis

Interconnect synthesis helps users to narrow down possible interconnect designs quickly. The domain of search is all processes/technologies that have been simulated in the batch-mode. The IPDA interconnect synthesis subsystem extracts a subset of designs that satisfy multiple performance goals such as impedance and noise margin specified by the user.

2.2.2 Viewing through X-Y Graph

The user can also look at the effect of changing trace width/spacing on any performance variable. This is done by showing any performance variable versus trace width and/or trace spacing. An arbitrary number of graphs can be generated so a user can simultaneously visualize trade-off for different trace width/spacing designs as well as their impact on several performance variables.

2.2.3 On-line Evaluation

An evaluation panel is provided for users to do stackup design. Stackup design involves assigning signal or reference planes to each layer of an interconnect construction. Once a user specifies layer assignment for a selected construction, IPDA can determine layer models for each layer. Furthermore, on-line performance evaluation can be done for each signal layer given the arbitrary trace width and spacing within the interpolation range.

To summarize for the use of interactive mode, users can interactively use interconnect synthesis, flexible X-Y graphing, and on-line evaluation simultaneously and iteratively to identify optimized interconnect designs in a timely fashion.

2.3 SPICE Generation and Simulation

With the scaling of MLITs, the multi-line busses carrying high frequency signals can no longer be accurately analyzed through the lossless transmission line performance parameters since the line resistance is comparable to the line impedance [11]. Using the SPICE ladder circuit model, the capacitive and inductive coupling in the multiple transmission lines can be included in the simulation and the resistive loss can be included with serial resistance in the ladder circuit. RLC SPICE subcircuits/circuits are therefore automatically generated so that distributed RLC interconnect simulation can accurately predict lossy-transmission line effects. An option is available on the Evaluation worksheet so that a user can choose any signal layer and the corresponding RLC subcircuit/schematic is shown in Figure 5.

For MCM1, Stripline model, 2 traces, T/W = 50 µm,
T/S = 50 µm

```
# For MCM1, Stripline model, 2 traces, T/W = 50 µm,
T/S = 50 µm

.subckt sub 1 2 3 4 99 (length)
  r1 1 101 value = 1.64604 * length
  r2 3 103 value = 1.64604 * length
  l1 101 2 value = 2.72263e-07 * length
  l2 103 4 value = 2.72263e-07 * length
  k12 11 12 value = 0.133351
  c1g1 101 99 value = 7.244e-11 * length
  c1g2 101 99 value = 7.23925e-11 * length
  c2g1 103 99 value = 7.244e-11 * length
  c2g2 103 99 value = 7.23925e-11 * length
.ends
```

The above format is used for both stripline and microstrip lines. To correctly represent distributed RLC networks for accurate SPICE simulation for lossy transmission lines, the length of each segment should be less than 10% of the wave length of the highest frequency component of significance. In terms of equation, the number of segments "N" can be obtained from

\[ Z_{eff} = \sqrt{Z_1 Z_2} \] (4)

\[ P_{dL} = \sqrt{(L_{11} + L_{12}) (C_{11} + C_{12})} \] (5)

\[ P_{dR} = \sqrt{(L_{11} - L_{12}) (C_{11} - C_{12})} \] (6)

\[ P_{d_{eff}} = \sqrt{P_{dL} P_{dR}} \] (7)

\[ V_B = \left( \frac{C_{12} L_{12}}{C_{11} + L_{11}} \right) \left( \frac{2C_{p} P_{d_{eff}}}{T_p} \right) \Delta V_S \] (8)

for coupled line lengths from \( L_{cp} = 0 \) to \( L_{cp} = t_f / 2P_{d_{eff}} \) and

\[ V_B = \left( \frac{C_{12} L_{12}}{C_{11} + L_{11}} \right) \Delta V_S \] (9)

for coupled line lengths of \( L_{cp} = t_f / 2P_{d_{eff}} \) or greater.

\[ V_F = \left( \frac{C_{12} L_{12}}{2} \right) \left( \frac{L_{cp} P_{d_{eff}}}{T_p} \right) \Delta V_S \] (10)

where \( \Delta V_S \) is the driving signal transition amplitude.
where $L_{um}$ is the coupled line lengths and $c$ is the speed of light. The SPICE circuit representation for the same geometry is shown below. Here nine segments are required for simulating this lossy transmission line from Eq. 11 with 0.2 ns risetime, and 3 in coupling lengths.

[Circuit diagram with SPICE code]

$N \geq 10L_{cm}(\frac{0.35}{c})(\frac{\sqrt{f_{c}}}{c})$ (11)

The users CM set up different signal inputs, termination, and IPDA. To further simplify the example, output driver signal is represented by a single low-to-high pulse with 0.2 ns risetime and 40 $\Omega$ source resistance. Receiver is assumed to have a high input impedance. The distance between driver and receiver is required to be 8 cm on a MCM. Interconnect choices include stripline or microstrip coupler configuration on several MCMs with different dielectric thicknesses and with/without coatings. The goal is to achieve the maximum of 1 ns delay and 100 mV/V crosstalk possible. Figure 6 shows the schematic for the example with open-ended termination.

[Diagram showing circuit schematic]

To use IPDA to optimize the design in this case, first one will set up batch mode simulations for possible interconnect design configurations. Figure 4 shows several construction choices for the MCMs. There are polyimide and ceramic materials with dielectric constants of 4.0 and 9.0, respectively. Coatings of various thicknesses are available for microstrips. Also trace width ranges from 10 to 60 $\mu$m, and trace spacing ranges from 40 to 500 $\mu$m. The result of the batch mode simulation is the interconnect $R$, $L$, $C$, impedance, propagation delay, and crosstalk information in the database for surface microstrip, buried microstrip outer (with coating), and stripline configurations for various technologies.

Once the database is built, the user can use IPDA's performance browser and graphics capability to look at different curves of interest. Figure 7 shows the impedance vs. dielectric thickness. Figure 8 shows the crosstalk vs. spacing. With coating thickness ranging from 10 to 50 $\mu$m, microstrip impedance and crosstalk changes about 5% and 10%, respectively. Now we could enter impedance and noise margin goals in the synthesis worksheet as shown in Figure 9, and IPDA will return all the choices that satisfy the requirements. The user could then use the evaluation worksheet to do more detailed design by specifying layer assignments for the chosen MCM technology. Arbitrary choices of trace width/spacing, coupling length, and risetime can be specified, and performance information can subsequently be derived. Figure 10 shows this example on the evaluation worksheet.

By choosing a specific signal layer from the evaluation worksheet, the user can generate and simulate SPICE subcircuits/circuits through the interactive SPICE setup worksheet and HPSPIECE window. Figure 11 shows the waveform of near end and far end crosstalk for an open-ended terminated coupler.
IPDA helps designers to analyze and optimize interconnect designs in an interactive way, but this procedure certainly could be done automatically as well. However, most designers would like to understand the results and options. There are other design constraints such as cost, thermal management, power consumption, manufacturability, etc. that determine the final choice of a certain technology.

For this application example, an open-ended termination coupler has less power consumption than well-terminated coupler. The cost of 9.0 dielectric material is cheaper than 4.0 dielectric material and may as well satisfy performance requirements. Microstrip with coating is more manufacturable than striplines. It would be difficult to know all the constraints up front before you explore possible alternatives. Since we use a driver with 0.2 ns risetime and 4.0 k source resistance, an open-ended termination microstrip (with coating) coupler with length equals to 8 cm is used on a 4.0 dielectric material with T/W = 40 µm, T/S = 60 µm, and dielectric thickness equals to 20 µm. For this choice, the final performance result are 0.54 ns delay, and 31 and 61 mV reduced noise margin due to crosstalk and reflection for near and far ends, respectively.

![Figure 7. Microstrip impedances vs. dielectric thickness for Er = 4, T/W = 50 µm, and T/S = 50 µm.](image)

![Figure 8. Crosstalk vs. Impedance for Er = 4.](image)

Figure 7. Microstrip impedances vs. dielectric thickness for Er = 4, T/W = 50 µm, and T/S = 50 µm.

![Figure 9. Arbitrary performance goals can be input on the synthesis worksheet.](image)

![Figure 10. MCM1 on the evaluation worksheet.](image)

![Figure 11. The near and far end signal and crosstalk waveforms for an open-ended coupler.](image)

### 3 IPDA Customization

We have observed major disparities between the interconnect modeling methods of IC, MCM, and PCB designers. Even for the same MLIT design such as PCB, microwave engineers may use modeling techniques very different from digital system designers.

Although this paper primarily describes the electrical performance measures of IPDA, other MLIT measures such as electromigration design rules, thermal dissipation, manufacturability, and cost analysis are also very important. We therefore implement IPDA using a spreadsheet interface so that users can do customization by entering their analytic equations or empirical rules regarding reliability design, thermal management, cost, or other manufacturability measures. Although progress has been made [16], software that can provide a total solution for system-level cost-performance trade-off is still missing. We hope the continuous improvement of
IPDA can achieve this goal.

4 Conclusions and Future Directions

In this paper, we present an interconnect performance design assistant (IPDA) that provides a unified way for hierarchically analyzing and designing multi-level interconnect technologies (MLITs) including IC, MCM, PCB, via and lead attachment. IPDA provides three major functionalities to achieve this. First, for completeness and speed, combinations of the whole range of parameters (width, spacing) for possible interconnect configurations are numerically simulated or interpolated in batch mode and are saved into a data file for each MLIT of interest. Furthermore, batch mode simulation for a new interconnect configuration can be easily setup and run. Results are then automatically added to the existing database. Second, optimization of an interconnect design can be achieved interactively through the goal-directed interconnect synthesis given performance goals, flexible X-Y graphing, and fast on-line performance evaluation for arbitrary layer assignment of an interconnect structure with the user-specified risetime, temperature, width, spacing, and coupling length. Third, complete SPICE subcircuit/circuit generation and simulation for an interconnect structure including the layer assignment, risetime, width/spacing, and coupling length can be generated and simulated automatically for signal integrity analysis. Study of the chip to chip communication for optimizing driver, interconnect, and receiver design in terms of total delay, noise margin, etc. can be done much easier and quicker. Besides the functionality above, IPDA’s ease of use is also very important for its acceptance to engineers. We have implemented the user interface of IPDA using a spreadsheet running on UNIX [17], with the bulk work done in C.

Therefore, IPDA provides engineers with common access to company-standard interconnect models for the full hierarchy of MLITs. This makes the different levels of packaging design more compatible and eases the task of system interconnect simulation even within the same company. The current IPDA is our first step toward unifying the performance simulations of MLITs at our company. Following are some of the future work:

With the performance database, the task of system-level cost-performance trade-off dealing with the full hierarchy of packaging and various bipolar or CMOS off-chip driver/receiver models becomes feasible. IPDA database can be used not only for pre-layout system-level cost-performance analysis but also for schematic capturing and post-layout parasitic circuit extraction. However, both the database format and the layout extraction methods for the IC/MCM/PCB tools have to be modified before the interconnect performance extraction routines and database can be integrated and used.

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