Automatic Layout Procedures for Serial Routing Devices

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Abstract

Conventional automatic layout systems have been applied to MOS or bipolar devices. However, these systems cannot deal with certain features, e.g. signal serialization, in serial routing devices such as Josephson devices. This paper defines layout requirements and presents new automatic layout procedures for such devices. These procedures are based on "subnet partitioning". They can be applied to hierarchical design of both masterslice and custom logic LSIs. Experiments using 4-bit-full-adder circuits confirm their feasibility.

1. Introduction

Many automatic layout systems have been applied to MOS or bipolar LSIs [1][2][3]. Their fundamental algorithms are independent of individual devices. There is also little difference between programs for MOS and bipolar devices.

New devices have been developed to achieve higher switching speeds. Unfortunately, only a few will become part of the mainstream. Design automation will be indispensable for certain features of such devices when VLSIs using them are designed. This paper focuses on serial routing devices, particularly on promising devices such as Josephson devices [4][5]. One of their distinguishing features is signal serialization. That is, such devices must be ordered in a serial chain. Reference [6] describes a stand-alone wiring program to handle this feature. However, it does not mention another important feature, current direction arrangement. The program is independent of conventional DA programs for other devices.

This paper defines three layout requirements: (1) signal serialization, (2) termination resistor assignment, and (3) current direction arrangement. It presents a layout strategy based on "subnet partitioning" to satisfy these requirements. This strategy allows easy enhancement of conventional automatic systems. It applies to the hierarchical design of both masterslice and custom logic LSIs.

2. Layout Requirements for Serial Routing Devices

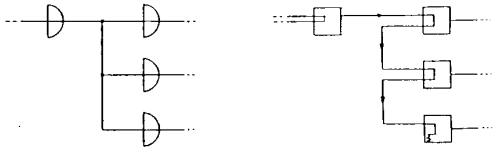
Serial routing devices such as Josephson devices have three layout requirements distinguishing them from conventional semiconductor devices:

(1) Signal serialization
(2) Termination resistor assignment
(3) Current direction arrangement

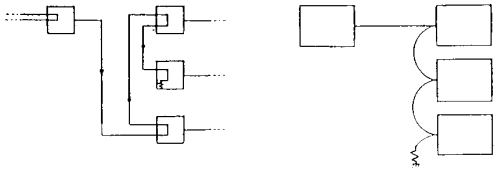
The difference in logic symbols between conventional devices and serial routing devices is shown in Fig. 1. In conventional devices, a logic input corresponds to a terminal. However, in Josephson devices, it corresponds to a pair of terminals. Since this logic operates according to current-driven flux, current goes into one terminal and out the other. A signal net must be routed serially with one stroke to obtain constant current. Moreover, a termination resistor must be assigned at the end of the serial wire to connect to ground. Routing models are compared in Fig. 2. Present semiconductor devices have no connection rule for signals in a chip. In Josephson devices, current flows from source to ground through the resistor. The serial length must be shorter, because signal delay is more severely constrained than in conventional devices. The length changes according to the route order (Figs. 2(b) and (c)). Thus the order must be chosen to minimize length. The serial routing model is quite similar to the routing model for ECL LSIs on PCBs (Fig. 2(d)).

(a) Conventional Devices (b) Josephson Devices

Fig.1 2-Input-OR Logic Symbols



(a) Conventional Devices (b) Josephson Devices



(c) Josephson Devices (d) LSIs on PCB

Fig.2 Routing Model Comparison

If the device symbol is regarded as an LSI, requirements (1) and (2) above apply to its routing problem. They differ in the terminal connection.

An example of physical terminal location corresponding to Fig. 1(b) is shown in Fig. 3. 1-1' and 2-2' pin pairs are mutually compatible. However, the current directions for 1-1'and 2-2' must be the same in order not to cancel the flux. When pins 1 and 2 are inputs, pins 1' and 2' must be outputs, and vice versa. This is called current direction arrangement. Pin assignment must observe this condition.

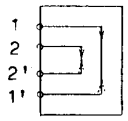


Fig.3 Current Direction Arragement

3. Layout Strategy

The new DA system for serial routing devices is based on enhancing conventional systems. The conventional system has been applied to both masterslice and custom logic LSIs. Moreover, it can handle LSI hierarchical structure [1], [2]. This paper presents the layout strategy for satisfying the three requirements in terms of its difference from conventional systems.

3.1 Basic Layout Flow

A basic flowchart of the layout for a serial routing device is shown in Fig. 4. The procedures are placement, subnet partitioning, and routing. Placement aims at minimizing total net length. Subnet partitioning includes signal serialization, termination resistor assignment, and current direction arrangement. Its evaluation function is defined by the serial net length. Each subnet is then routed. Conventionally, a manual layout designer simultaneously partitions a net and places cells to shorten its serial wire length. Partitioning makes manual layout more complicated than in conventional devices.

Three automatic layout methods based on subnet partitioning are possible to improve manual layout results:

(a) Subnet partitioning just after placement
(b) Subnet partitioning just before placement
(c) Subnet partitioning in logic description

(a) has two advantages. Subnet partitioning is easily optimized according to cell placement (see section 4 below). Moreover, the placement process handles each net and places cells connected to a net closer together. (b) and (c) have disadvantages. The available objective function in partitioning cannot be defined since length estimation precision is too low before cell placement. It is also difficult to place cells according to expected cell location in subnet partitioning. Furthermore, logic simulators and other DA subsystems are not available for (c), when the logic itself is changed. This contradicts the stated goal of making maximum use of conventional systems. Thus method (a) is chosen. Each subnet is then routed.

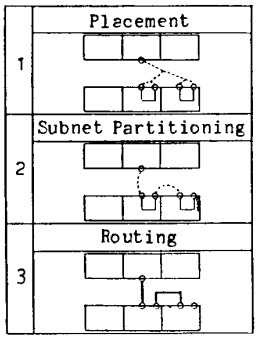
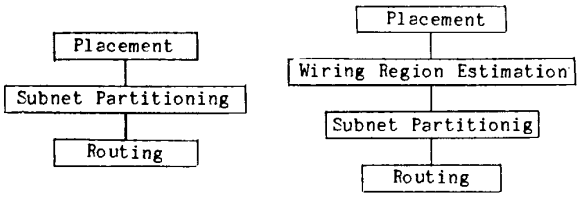


Fig.4 Layout Flowchart

3.2 Masterslice and Custom Logic LSIs

Layout flows are compared in Fig. 5. In masterslice LSIs that limit cell location to a fixed area, cell location is definite after placement. After cell and pin location are determined, the net is partitioned into two-pin subnets to minimize its total length. The router then deals with these subnets.

By contrast, in custom logic LSIs, cell location is not determined even after placement is finished, since the wiring region varies with routing. That is, the wiring region's horizontal size is fixed, but its vertical size changes with routing. Thus a cell location estimation process is necessary to perform subnet partitioning. The difference from masterslice LSIs is that cell location is estimated by routing nets for subnet partitioning. Nets are then partitioned according to the estimated cell locations. The subnet partition, like the maze router, requires definite cell location.



(a) Masterslice LSI (b) Custom Logic LSI

Fig.5 Layout Flow Comparison

3.3 Hierarchical Structure

The chip consists of block regions, blocks, and cells (Fig. 6). The programs for intrablock placement, intrablock routing, interblock placement, i.e. floor planning, and interblock routing have been applied to this chip hierarchy. In serial routing devices, some parts of a net in a block can be partitioned after intrablock placement, since the intrasubnet length is generally shorter than the intersubnet length.

However, the parts that are enclosed in an upper block region cannot then be partitioned (Fig. 7). Thus they can be partitioned after interblock placement because of definite cell pin location. This condition is analogous with the need for absolute block location with interblock routers like the maze router. Finally, interblock routing is performed for pin-to-pin subnets.

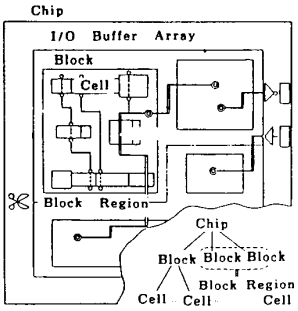


Fig.6 Hierarchical Structure of Chip

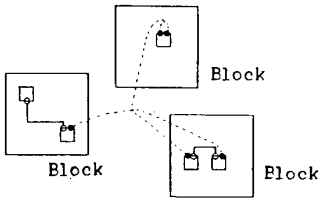


Fig.7 Interblock Net

4. Layout Algorithms

4.1 Subnet partitioning

The subnet partitioning procedure guarantees that the three layout requirements are satisfied. It aims at minimizing serial net length. Since subnet partitioning is performed after placement, cell and cell pin locations are definite. The procedure includes three steps: subnet partitioning, current direction arrangement, and termination resistor assignment (Fig. 8).

(1) Subnet Partition

The subnet partitioning problem is theoretically equivalent to the Traveling-Salesman Problem. Consider a net having n pins. A salesman leaves his home city (source pin) and visits all other cities (sink pins) without returning to the starting point. The total cost is the sum of the Manhattan distance between cities (pins). The solution is the shortest route. This famous problem is NP-complete. However, the optimal solution can be obtained by enumerating all the combinatorial cases for $n < 10$, since $n = 9$ has about 400,000 cases, which is small enough to be handled by a large computer. For $n > 9$, several heuristic algorithms [7], [8] are provided and the best solution is chosen. Here, computing time can be reduced by reducing the number of pins to be handled. A terminal pair corresponding to a logic input can be approximately regarded as a pin if the distance between its pair is less than the net length. This condition is generally applied to intrablock subnet partitioning. The representative pin is located at the midpoint between its pair (Fig. 9). The number n of pins is defined as

$n = Tk / 2 + 1,$

where Tk is the number of sink terminals. Thus the threshold, $n = 9$ corresponds to $Tk = 16$.

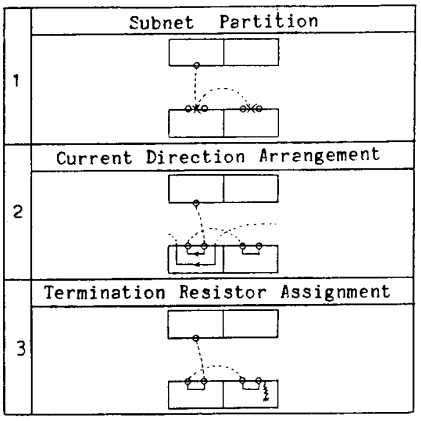


Fig.8 Flowchart for Subnet Partitioning Procedures

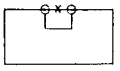


Fig.9 Representative Pin

(2) Current Direction Arrangement

Although the current directions of intersubnets are fixed, those of magnetically coupled signals are checked for each cell in a block. If a violating cell is found, its terminal pairs are exchanged. The objective function is to minimize elongated length.

(3) Termination Resistor Assignment

The termination is assigned at the end of the wire. It can be selectively incorporated into each cell.

4.2 Placement and Routing

Both placement and routing algorithms have been developed for CMOS and bipolar devices [1]-[3]. In intrablock placement, a two-dimensional clustering algorithm is used for initial placement, and net balance and pairwise interchange for iterative improvement. Subnet routing and net prerouting for estimated cell location use the same routing algorithm, i.e. a channel router, in intrablock routing. Iterblock routing is performed with the maze router.

5. Experimental Results

The programs developed as described in Sections

3 and 4 are incorporated into one of Hitachi's conventional DA systems. They are written in FORTRAN, and run on the Hitachi M280H using the VOS3 operating system. Experiments have confirmed feasibility. This new additional DA system is applied to 4-bit-full-adder circuits consisting of Josephson devices as an example of serial routing devices. The experimental data and chip are shown in Table 1 and Fig. 10. The next paper will describe performance in detail.

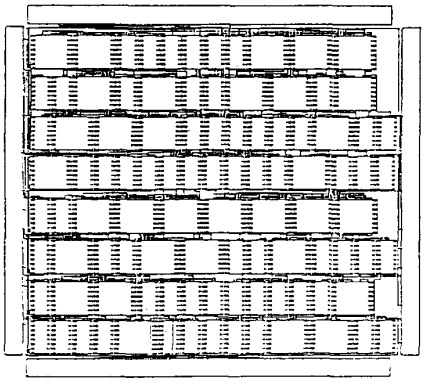


Fig.10 Chip Layout Drawing

Table 1 Data Specification

No. of Cells			No. of Nets	No. of Terminals		
OR·AND	OR	Total	Total	Total	Average	Maximum
33	66	99	118	545	4.6	33

The chip consists of an internal block and four surrounding blocks. Internal intrablock layout is generated automatically. Interblock placement is then determined interactively using a floor planning program.

6. Conclusion

New automatic layout procedures for serial routing devices such as Josephson devices have been presented. The layout of these devices is characterized by (1) signal serialization, (2) termination resistor assignment, and (3) current direction arrangement. Subnet partitioning is a key to satisfying these requirements. The basic layout procedures are placement, subnet partitioning, and routing. Subnet partition that serializes signals is equivalent to the Traveling-Salesman Problem, which is NP-complete. However, all cases can be enumerated in each net having fewer than 16 sink terminals. Conventional heuristic algorithms are used in the others. Given definite cell location, subnet partitioning produces near-optimal results. It is analogous with the maze router in its need for absolute cell location. A layout strategy applicable to the hierarchical design of both masterslice and custom logic LSIs has been presented based on the above conditions. When cell location is not definite, it is determined by wiring region estimation.

Experiments have been performed for 4-bit-full-adder Josephson circuits. The developed programs have been incorporated into a Hitachi conventional automatic layout system. The results confirm feasibility. Performance is now being evaluated.

7. Acknowledgements

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