CAN CAD MEET THE VLSI DESIGN PROBLEMS OF THE 80's?

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I feel we should be very optimistic that future CAD will enable cost-effective device designs as process geometrics continue to scale downward. Obviously, CAD in the 80's will be significantly different than CAD in the 60's and 70's. We will experience a transition which will focus emphasis on the management of design complexity and higher-level forms of device design in an effort to maintain competitively acceptable levels of designer productivity. Also, the influence of color graphics, microprocessors, telecommunications, and distributed computing concepts will have a profound impact on VLSI device design methodology.

The enormous increase in device complexity anticipated with VLSI, will demand conceptual and algorithmic innovations in digital-analog simulation and circuit analysis. It is rather obvious that continuous increases in model size, number of logic gates and circuit nodes, causes an exponential increase in computer costs associated with exercising the model in generating analytical behavior. Therefore, more cost-effective algorithmic techniques and hierarchical methods must be developed for VLSI digital-analog simulation and circuit analysis. Another extremely perplexing design problem is device testability. If built-in test (BIT) techniques, which appear very promising, are developed, it will impact future device architecture and test synthesis methodologies. CAD must be a partner in catalyzing these technological changes.

Hierarchical design techniques appear to provide the best foundation for structuring a VLSI device design methodology. This implies that the complex device design will be partitioned into more manageable parts; these parts shall be referred to as building blocks. These building blocks will be synthesized in parallel utilizing an interactive symbolic layout design technique; this is a high-level form of layout design pioneered by Rockwell International. The addition of interactive color graphics to this symbolic layout design technique promise some provocative enhancements that should be beneficial in VLSI device layout design. Following design verification and analysis of each building block, they will be analytically assembled to form the complete device design and transformed into numerical control data for photo, e-beam, or x-ray lithographic processing.

The technical challenges associated with VLSI will provide a very exciting CAD development environment in the 80's. Even though these CAD challenges appear formidable in regard to today's technology plateau, I am extremely confident the innovative and competitive forces of our microelectronics industry will provide a cost-effective VLSI device design methodology in the 80's.