VLSI technology is rapidly approaching a million devices per "random" logic chip. The potential complexity of such chips will exceed the ability of humans to organize and layout the silicon, and bring out a product in a competitive and timely market position.

Traditional computer aided layout techniques will flounder and low layout densities and/or excessive computer costs, and the fast changing technology will obsolete all library data almost as soon as it is used (or before).

Can man and computer combine to meet these problems? At this time, such techniques have not produced designs that are as competitive and timely as man alone. Will the complex designs of the future change that? Are there tools and techniques being developed today that can be used to meet the challenges of the 80's, or are we developing tools for an obsolete design methodology, and what tools should be developed instead?

PANEL: Dan Schweikert Bell Labs
       David Giuliani Hewlett-Packard
       Rox Waxman IBM
       Bill Lattin Intel
       Warren Wiemann Motorola
       Robert Larsen Rockwell
       David Hightower Texas Instruments

*Panel members have been asked to submit a one to two page response or rebuttal to the above statements, and prepare a three to five minute talk summarizing their position.