Welcome to the 13th annual Symposium on Hot Interconnects! This conference brings together designers and architects of high-performance switching chips, routers, and packet processing circuits from universities and industrial research laboratories. Presentations focus on up-to-the-minute developments demonstrating leading-edge designs and their performance evaluations by engineers and researchers throughout the world.

Thanks are due to the program committee for their hard work in reviewing the papers and selecting the material that appears in this conference. Each member of the technical program committee reviewed four to six papers and provided valuable feedback to the authors. Each paper received at least three reviews.

This year 40 papers were submitted, of which 12 were unconditionally accepted. An additional four papers were conditionally accepted and were successfully shepherded by members of the TPC. We accepted four papers as short papers.

The technical program is organized into five sessions of full papers, plus a session for short papers to be presented in a poster session during the conference. These sessions cover recent advances in high-performance networks for supercomputers, network processors and associated technologies, and high-performance routers, and provide in-depth performance evaluations of the latest research and industrial prototypes.

The conference will begin with a session on recent advances on interconnection networks for supercomputers. Papers in this session describe proximity communication, a revolutionary technique for addressing the bandwidth bottleneck in chip-to-chip communication; highly scalable collective communication protocols implemented on one of the most powerful supercomputers in the world, ASC Thunder; a new generation of low-latency optical switches jointly developed by Corning and IBM based on optical cell switching with electronic control; and the architectural design of the new IBM HPS family of high-performance switches and adapters.

The next session will provide performance evaluations of Infiniband, Gigabit Ethernet, and the Cray Seastar interconnect. The first study quantifies how communication protocols can benefit from a fast SDRAM memory in the network interfaces. The other two studies describe the basic performance of the Cray Seastar interconnect and the performance implications of an off-load engine in the Chelsio 10-Gigabit adapter.

The third session will explore network processors and associated technologies. This session will include three papers; two of them describe a content-aware switch using a network processor, a hybrid cache architecture for high-speed packet processing. The third paper describes a high-speed, low-power network search engine using an adaptive block selection scheme.
The fourth session will showcase high-performance routers. This session will include three papers, one describing a scalable switch for service guarantees, another the design of randomized multi-channel packet storage for high-performance routers, and the third addressing queuing bottlenecks in high-speed routers.

The papers in the fifth session provide an insightful discussion on how TCP is implemented on the latest family of Mellanox Infiniband adapters, describe the architecture of an intrusion filter for TCP, and detail the internal design of a buffered packet switch.

**Short Papers** In additional to the general papers in the conference sessions we accepted five short papers. These papers will not be presented in the main sessions, instead the will be presented as posters in the main lobby. Some of the posters will also include live demos. These papers describe distributed grid topology discovery, a terabit-capacity photonic interconnection network, a study of InfiniBand in a lossless network, an ultra-low latency approach for InfiniBand, and reconfigurable network hardware.

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