FREACS — A Fast REflection And Crosstalk Simulator

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Abstract: In this paper we present the new simulator FREACS for the transient analysis of single and coupled transmission lines. The simulator is part of an EMC-workbench concept.

The design of FREACS differs from the usual implementations. For example new macromodels of digital circuits as transmission line terminations are used.

A formal input language called TANDEL was developed for the description of transmission line circuits.

The simulation of a complex transmission line circuit will be discussed as an example. Further the calculation time of the simulator will be compared to the circuit complexity.

Introduction

With the application of new electronic devices, the practice has shown that the electronic and layout designers are desperately in need of assistance, by means of new tools for printed circuit board design with respect to EMC problems. Such a requirement originates in the increasing processing-speed of devices based on new IC technologies (ACMOS, HCMOS, BICMOS, etc.) as well as in the highly packed structures of printed circuit boards. On printed circuit boards problems arise, particularly through thermal and electromagnetic coupling.

In this paper the problem calculating the effects from electromagnetic coupling will be discussed. During the process of a printed circuit board design, the electronic and layout designer has to account for various effects, such as reflection, crosstalk, simultaneous-switching, current-spikes, and radiation of electromagnetic energy.

In many cases it is not possible to detect such errors, which were caused by noise effects, before the prototype has been tested respectively the product has been analyzed at customers through the field service.

The first instance may lead to a prelarged design cycle and possibly to excessive efforts during the testing period whereas the secondly mentioned would most certainly conjure up regarding the deficient product quality.

In order to decrease the above stated excessive design efforts in the future, it will be necessary to recognize such problems at an early design stage.

The above mentioned noise effects are not to be seen as isolated occurrences, but have to be accounted for as attributes of a specific design.

Conclusively the respective design procedures have to be altered.

To achieve this necessity, not only the EMC-departments have to make sure the compliance of the printed circuit boards with the EMC requirements. It will also be necessary to include EMC-oriented analysis and development methods at an early design stage by the electronic and layout designers themselves.

It is of a great importance to fulfill this demand because of the effect that the application of measuring techniques, in scope of an EMC-suitable analysis, is set within certain limits.

Because of highly packed structures on current printed circuit boards and the lack of available space, it is not possible to record all of the effects mentioned above by measurement.

The consideration of EMC-effects during a design process of electrical and electronic components will be a highly complex design task. The reason for that is the necessity to combine the so far established design procedures with the EMC-appropriate design methods.

To solve EMC-problems on component level the provision of calculation methods which are based on the application of scientific methods, is essential and indispensable.

This will be the only way to push aside the influence of so-called 'Black-Magic-Effects', which often predominates the design methods under EMC aspects.

It becomes obvious that the complexity of the design task and the tools supporting the design of components under EMC-constraints needs the use of CAE methods.

A Concept for an EMC-Analysis System

A refined and already realized concept for the EMC-appropriate printed circuit board design will be presented as follows (see figure 1). Based on the layout design, direct and indirect subnets are extracted with the assistance of the layout data extractor (LDE) and a suitable device description. Here a direct subnet consists of transmission lines that are exclusively connected with each other by electrical contacts. Concerning the indirect subnets, these are additionally influenced by the electromagnetic field of adjacent transmission lines.

The succeeding layout data analyzer (LDA) reduces the number of the subnets to a less number of critical subnets. Ultimately only the critical subnets have to be reviewed, by means of a further extensive analysis on the electromagnetic compatibility of a component.

Call upon the results of such an analysis, proper EMC-measures can be introduced in order to abolish or at least to minimize the ascertained effects and their impact. It has to be noted that only local modifications of the actual layout design should be made under such measures; otherwise additional problems may arise from different locations of the layout.

Subnets which are evaluated as 'critical' will be transformed into an adjusted description for the simulators (FREACS [7], SPICE [1]), with the application of the 'input-generator'. The necessary transmission line parameters (characteristic impedance, inductance- and capacity matrices, phase velocity), can be determined through the application of the TALC program [10].

Depending on the desired accuracy of the analysis and the specific application, either the FREACS simulator or the SPICE simulator may be used.

The detailed analysis of a circuit, for instance a driver gate in connection with application on a printed circuit board, requires the usage of the SPICE simulator. Only in the case that this requirement is obeyed, the analysis of voltage curves on the inner nodes of the gate circuit will be possible.

The analysis of complex transmission line networks with SPICE is not always possible.

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Figure 1: Concept for an EMC-analysis system

PCB-layout design
LDE (layout data extraction)
Device library
device library
TALC
Input generator
LDA (layout data analysis)
TALC
input generator
Macro model
FREACS
SPICE
Preprocessor
Output
Analyzer
Figure 1: Concept for an EMC-analysis system

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In the instance that the line terminations can be described by macromodels, complex transmission line networks have to be investigated, and a considerable reduced calculation time is required, the FREACS simulator will be applicable.

The representation of the simulation results can be shown with the tools DIAG/PLAS and AnaRes [5]. It is also possible to present the simulation results by lists or plots. Furthermore it is within the bounds of possibility to display and analyse the results directly on a graphic screen.

A detailed description of simulator attributes will be given in the following.

The Simulator FREACS

By virtue of the FREACS simulator the user is able to analyze the reflection and crosstalk behaviour of transmission line subnets on printed circuit boards. A subnet consists of transmission line areas and their termination networks.

A transmission line area consists of single or parallel coupled transmission lines of equal length. Thereby a quasi-TEM wave-propagation is assumed. With this assumption the 'model of delayed current components' can be derived, describing lossy [11] and lossless [7] transmission lines. This model consists of resistive networks and controlled current sources.

In high speed applications the influence of transmission line discontinuities has to be considered as well. A method for the simulation of discontinuities was introduced in [9].

A termination network can consist of input and output stages of gates, resistors and a number of different components. If termination networks consist either fully or partly of gates, it will be possible to use macromodels especially developed for the simulator [8]. A special library contains the data concerning the model description.

To simulate the subnets it is possible to arrange a special partitioning of the transmission line structure because of the delay time behaviour of transmission lines. The special algorithms applied in FREACS were already introduced in [7]. In the following, only the structure of the simulator and the input language will be explained.

Structure of The Simulator

A simulation run, analyzing a subnet, is started by reading the corresponding input file. The input file contains the complete transmission line network description and the necessary control statements that are described by a specially developed formal language (TANDEL, Transmission Line Network Description Language).

An input parser checks the file for syntactical as well as semantical errors. Note, that a check on semantical errors is extremely difficult and not possible in every case.

After the input file is read in without errors, a preprocessor transforms the internal circuit description into the internal data structures of the simulator. For example the constant parts of the admittance matrices for the nodal analysis and the corresponding tables for the voltage values of a subnet will be set up.

Using the delay-behaviour of the transmission lines, the voltage- and current values at the two ports of each line area can be determined independently. As a consequence of this fact, it is not necessary to simulate the complete subnet with the shortest delay time of the transmission line system. The partitioning of the line system requires the use of a synchronization-algorithm.

The solution of linear termination networks is carried out using a solver for linear equations, whereas the non-linear termination networks are solved with the help of the Newton-Raphson algorithm.

The calculated voltage waves are filed in DIAG format into output files. Figure 2 displays the simulation flow graphically.

The program system FREACS is written in the language C. Consequently a dynamic memory management could be implemented. There was no necessity to develop a so called 'memory manager' as it would have been the case if languages were used that allow fixed dimensioned fields only. In this way the field dimensions are adapted to the required data dynamically. Also an optimized exploitation of the required memory is guaranteed. By virtue of the development of a special administration algorithm it is sufficient when only the necessary voltage and current values to simulate the delay time behaviour of transmission lines are buffered into appropriately dimensioned fields. The voltage and current values which are not required for the calculation at the actual time point are deleted. Because of a continuous output of each required voltage wave into files the creation of appropriately large dimensioned fields in the main memory is avoided.

The Transmission Line Network Description Language TANDEL

The formal input language called TANDEL was developed specifically for the transmission line simulator FREACS. The input language is highly flexible in regard to the network description and a possible grammar extension. The structuring of the network description in main- and subsections gives a better understanding and a good legibility of the program text. The complete input file contains the description of a transmission line network, the termination networks including the definition of macromodels and stimuli, and the control statements. The structure of an input file will be described briefly in the following.

Structure of the Input File

The sections are identified by keywords in the following way:

- MODELDEFS: this section contains the definition of the different types of macromodels which are present in the subnet.
- NETLIST: this section describes the network structures of the subnets.
- CONTROL: this section contains detailed informations to control the simulator.

The NETLIST-section and the CONTROL-section are divided into subsections. The contents of the subsections can be recognized by the use of fixed keywords.

The analyzed network has to be sub-divided into transmission line areas and termination networks. In the NETLIST-section, the different transmission line areas and termination networks and their connections are represented. This section is divided into four subsections:

- transmission line section (AREA): transmission line areas consist of a single or parallel coupled transmission lines of the length $l_k$. The electromagnetic properties do not change within a transmission line area.
- termination section (TERM): terminations are networks of resistors, capacitors, inductivities, current and voltage sources, and input or output stages of gates.
- discontinuity section (DISCON): this section describes junctions or other discontinuities by use of appropriate parameters. Note, that this feature has not yet been implemented into the FREACS simulator.
- linking section (CONNECT): the nodes which connect the transmission line areas, the termination networks and discontinuities are listed in the CONNECT-section.
The CONTROL-section is divided in three subsections as follows:

- analyse-section (ANALYSE): this subsection contains the information controlling the analysis type, the total simulation time and the maximum time step width.
- output-section (OUTPUT): in this subsection the output-files which contain the voltage curves, are specified.
- option-section (OPTION): the optional values controlling the simulation are listed in this subsection.

Examples of Semantical Errors

As mentioned above, the input parser checks the input file for syntactical and semantical errors. In this section, a list of some detected and not detected semantical errors will be given.

Detected semantical errors are:

- double named network elements like line areas, termination networks, stimuli, resistors etc.
- non-connected line areas and termination networks
- citation of a macromodel that is not defined
- wrong data for the dimension of line areas, length of line areas, node number of termination networks (less number than really defined)

Not detected semantical errors are:

- wrong data for the node number of termination networks (higher number than really defined)

If the input parser detects an error, an error message will emerge in the protocol-file. The error message includes the line number of the detected error in the input-file and a description of the error. Figure 3 shows an example of an error in the input file and the corresponding error message.

```
9 area ar0
10 line = 0;
11 dim = 2;
12 len = 15cm;
13 cmat (5.162008e-11 -1.113087e-11
14 lmat (6.994714e-7 2.019546e-7
15 >
```

Error Message:

```
[Error 1] line 12 near ';': check dimension
```

Figure 3: Example of a semantical error

Example

In figure 4 a subnet is displayed that consists of five transmission line sections and four termination networks. Driver and receiver gates in HC technology were chosen. In this example measures reducing the crosstalk effects will be studied.

![Figure 4: Arrangement analyzing crosstalk-effects](image)

Figure 4: Arrangement analyzing crosstalk-effects

First an arrangement without a shield line will be examined. The driver circuit NET1 is silent, whereas the NET2 will be controlled by the signal STIM2 starting at 15ns and with the duration of 10ns. In this case antiparallel crosstalk occurs. Figure 5 shows a part of the input-file for the subnet in figure 4. The sections of the subnet (line areas and terminations) that are not listed, are defined accordingly.

```
netlist{ area AR1 line = 0;
10 len = 16cm;
11 cmat (5.162008e-11 -1.113087e-11
12 lmat (6.994714e-7 2.019546e-7
13 >
```

Figure 5: Listing of the input file

In order to reduce the crosstalk effect the insertion of a shield line, the decrease of the coupling length, and the increase of the distance between the signal lines are different possibilities.

Table 1: Maximum amplitudes of the coupled noise voltage depending on $l_k$ and $s$ (without shield line)

<table>
<thead>
<tr>
<th>coupling distance $s$ (mm)</th>
<th>$l_k$ = 5 cm</th>
<th>$l_k$ = 10 cm</th>
<th>$l_k$ = 15 cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>1.12</td>
<td>1.5</td>
<td>1.95</td>
</tr>
<tr>
<td>0.6</td>
<td>0.86</td>
<td>1.18</td>
<td>1.58</td>
</tr>
<tr>
<td>0.9</td>
<td>0.68</td>
<td>0.95</td>
<td>1.27</td>
</tr>
</tbody>
</table>

Table 1: Maximum amplitudes of the coupled noise voltage depending on $l_k$ and $s$ (without shield line)

```
coupling distance $s$ (mm) | $l_k$ = 5 cm | $l_k$ = 10 cm | $l_k$ = 15 cm |
-----------------------------|--------------|--------------|--------------|
 0.3                         | 1.12         | 1.5          | 1.95         |
 0.6                         | 0.86         | 1.18         | 1.58         |
 0.9                         | 0.68         | 0.95         | 1.27         |
```

Figure 6: Transmission line configuration
Analyzing the influence of the shield line, the configuration shown in figure 6 is used. The line parameters (L- and C-matrices) of the coupled line section are determined for a two-coupled line system considering the shield line \( L_{55} \) connected to ground.

The transmission line parameters could be determined by the program TALC. When a shield line is inserted an enormous reduction of the coupling noise is assumed (see table 2).

\[
\begin{align*}
\sigma_1 & =\sigma_2 = 0.3 \text{ mm} \\
\omega_1 = \omega_2 = \omega_3 = 0.3 \text{ mm} \\
L_2 & = 5 \text{ cm} \\
L_3 & = 10 \text{ cm} \\
L_4 & = 15 \text{ cm} \\
V_{\text{m}}, [\text{V}] & = 0.175 \\
V_{\text{m}}, [\text{V}] & = 0.25 \\
V_{\text{m}}, [\text{V}] & = 0.3
\end{align*}
\]

Table 2: Maximum amplitudes of the coupled noise voltage depending on \( I_k \) (with shield line)

In figure 7 and 8 the simulation results with a coupling length \( I_k \) of 10 cm are on display. The influence of the shield line in the coupling area concerning the coupled noise \( v_2 \) is shown in figure 7. The voltage \( v_4 \), considering a shield line, is similar to the voltage \( v_4 \) without a shield line.

![Figure 7: Voltage \( v_2(t) \) (with (+) resp. without (O) shield line)](image)

![Figure 8: Voltage \( v_4(t) \) (with (+) resp. without (O) shield line)](image)

Calculation Time Compared to the Circuit Complexity

Now, we investigate the calculation time of the simulator FREACS as a function of the complexity of the transmission line configuration. In figure 9 the structure of the test-circuit is shown.

![Figure 9: Structure of the test-circuit to analyse the influence of the complexity of the transmission line configuration](image)

The driver-circuit and the receiver-circuit consist of linear and non-linear elements, such as voltage sources, macro-models, resistors etc. Their structures will not be changed, whereas the structure of transmission line configuration will be changed by the following aspects:

- number of connected transmission line sections \( n \)
- length of each transmission line section
- coupling of the transmission line sections
  - 4 single transmission lines
  - 2 two-coupled transmission lines
  - 1 four-coupled transmission line

In figure 10 the calculation time is shown which is necessary to simulate the structure of figure 9 depending on the length of the sections. The simulations are performed by a SUN SPARCstation 1+ (16 MIPS).

![Figure 10: Calculation time as a function of the number of transmission line areas](image)

We can now see, that the calculation time depends on the line-length in the case of four-coupled lines. In this case the number of line sections strongly influences the calculation time. If single transmission lines are used for the description of the line sections the influence of these aspects will be of inferior importance. One explanation for these relationships is, that in the case of single transmission lines the termination networks at each line will be solved independently, whereas in the case of coupled lines the whole network has to be solved. The phase velocity, respectively the delay time of the propagation modes of the transmission line sections, also influences the calculation time.

Another aspect influencing the calculation time is the complexity of the termination networks. The used stimulus of the driver-circuit is also an important factor. The configuration which is investigated at first consists of one four-coupled transmission-line section with a line length of 5 cm. The same model is used as driver-circuit for each line of the transmission line section. Linear voltage- and current-sources are used as well as nonlinear driver models for ALS, HC- and AC-gates. The receiver-circuits of the previous example are used. In figure 11 the calculation time is a function of the used driver-model and the used stimulus.

![Figure 11: Calculation time as a function of the driver model and stimulus](image)
Next, the receiver-models will be changed whereby the original driver-circuit will be used. The transmission line section of the last example is chosen. The same receiver-circuit is connected to each line of the transmission line section. Figure 12 shows the different receiver-circuits.

Figure 12: Receiver-circuits

A cascade of the receiver Rec2 will also be used, showing the influence of an increase in the number of nodes of a termination network. The calculation time as a function of the used receiver-network is shown in figure 13.

Figure 13: Calculation time as a function of the receiver-circuit

Summarizing the effects of termination networks we can say, that the use of linear circuits leads to less calculation time than the use of nonlinear circuits. This fact follows directly from the different methods solving the network-equations. The number of nodes of the termination networks influences the calculation time as well, see the previous example. Another factor is given by the used stimuli. High activity (many impulses, short impulses) increases the calculation time whereas low activity decreases it.

Conclusions

A fast simulator to analyze reflection and crosstalk noise on transmission lines with non-linear terminations was described. For the description of transmission line circuits the input language TANDEL was presented. The application of the simulator was demonstrated. Further investigations relative to the performance of FREACS were carried out.

The simulator is part of a concept for the design of PCB’s with consideration of EMC problems. This concept is based on the fact that current CAD-tools already applied in many electronic departments can still be used.

Within the framework of further developments FREACS is a integrated part of an EMC-workbench. The work of integration in the continuation has to give priority of any further activities. Furthermore, it is necessary to focus on the problem connected with the setup of an EMC-library. Especially larger sets of macromodels, dedicated to different IC-technologies, have to be provided. This topic leads to an extension of the FREACS application domain.

Literature


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