RISC AND ASIC – THE TECHNOLOGIES OF THE NINETIES

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Abstract
Again ASIC is the innovative technology in the microelectronics world, witnessing an implementation of RISC microprocessor architecture in a fully integrated complex system solution. In benchmark studies the RISC 32-bit architecture offers higher performance than conventional 32-bit microprocessors. This higher processing power is achieved by streamlining the instruction set to the most important and regularly used instructions in an architecture which executes these instructions in one machine cycle and at the same time using a pipeline structure. RISC microprocessors are implemented typically in high performance computers, workstations and embedded control real-time systems. The next generation of system implementation will combine RISC microprocessors and ASIC technology on one chip for easy migration to newer technologies as they arrive. Not only does it allow for increased speed of the processor but for high systems integration including a significant amount of functionality which improves the system performance. In order to be able to design an ASIC-based integrated system with a complexity of more than 100,000 gates on one chip, including the core of a microprocessor and at the same time developing the application program it is absolutely vital to provide the system designers with comprehensive and highly sophisticated CAD tools. These tools maximize the designer’s potential to develop his system in a "top-down" approach from an abstract behaviour description down to a detailed gate level.

RISC – Its Advantages and its Future
The microprocessor arena is currently witnessing a revolution leading to an enormous success of RISC processors (Reduced Instruction Set Computing). Other than processors based on the CISC principle (Complex Instruction Set Computing), RISC-based microprocessors have an architecture restricted exclusively to the most frequently used instructions. This approach has several advantages. First, a 32-bit RISC processor requires significantly less chip area than a 32-bit CISC processor based on comparable technology. Second, the 32-bit RISC processor’s computing power surpasses the performance of its CISC equivalent by a factor of up to five. Thus, RISC technology allows the integration of a maximum amount of processing power on a minimum amount of chip area. Due to the advantages of the RISC processors mentioned above, these products...
will feature outstanding growth rates in a wide spectrum of markets in the years to come. Among these markets are the telecommunications sector, data processing (including high-performance workstations, graphics and image processing), real-time control systems and embedded controllers, and top-performance computers for aerospace and military applications. An open architecture is the main element of the two popular RISC concepts developed at Berkeley and Stanford. Both are easy to implement in connection with ASIC's. This concepts have been implemented by MIPS and SUN, respectively.

MIPS
The MIPS family consists of the CPU's LR2000 and LR3000, each of them complemented by an on-chip Memory Management Unit (MMU), a Cache Controller and a Translation Lookaside Buffer (TLB) for fast translation of virtual addresses into physical memory addresses (see figure 1). In addition, the family consists of the Floating-Point Accelerators (FPA) LR2010 and LR3010 which act as co-processors and are designed for IEEE 754-1985 format, and the Write Buffers LR2020 and LR3020 which make up the interface between the high-speed cache and the slower main memory.

SPARC
The SPARC family consists of the Integer Unit (IU) L64801 (see figure 2), the Floating-Point Controller (FPC) L64802 acting as the interface to the floating-point co-processor, and the Memory Management Unit (MMU) L64803. Future upgrades towards a higher degree of integration (e.g. a combination of the MMU and the cache controller or the FPC and the FPC) have already been taken into account.

ASIC - Its advantages and its Future
ASIC technology is the driving force for the dynamic development in microelectronics. This has been the case in the past 8 years and will be continuing in the future. ASIC design methodologies and CAD tools have revolutionized the way circuits and systems are designed. While glue logic comprising around 500 gates was mainly implemented at the beginning of the 80's, entire systems with complexities between 100,000 and 200,000 gates are implemented on a single chip today. In addition, state-of-the-art sub-micron CMOS technologies today reach gate propagation delays of less than 500 ps. As a result of all this, ASIC's are the fastest growing market segment of the semiconductor industry, and all market analysts agree that this situation will continue in the future.

RISC and ASIC
ASIC's are the fastest growing market segment of the semiconductor industry, and RISC microprocessors feature the highest growth rates in the microprocessor sector. Future development of ASIC's is process-driven, while architecture and software are the driving forces for RISC processors. Thus, a combination of the best architecture, the best processes and the best software is unbeatable.

The RISC products mentioned above are available as standalone products. Starting in 1989, the selection of RISC components will be available as cores for the implementation of ASIC's. Using the LCB007 family, the system designer will thus be able to implement a RISC processor core together with the MMU, the Cache Controller, the Write Buffers and additional peripheral functions on one chip (see figure 3), but he will have the option to customize the processor core itself. Silicon development is accompanied by software advances. The MDEm CAD package will be complemented by system programming software.

Figure 3:
so that the system designer will be able to develop hardware and software together, on one system and in a coordinated manner (see figure 4). Consequently, the combination of RISC and ASIC is offering the system designer the highest performance at a drastically shortened development cycle, yielding an optimum price/performance ratio.

Figure 4:

![Diagram showing the process of design definition, software development, hardware development, software test and debug, hardware test and debug, and hardware and software integration.]