ABSTRACT The trends in VLSI / ULSI technologies are outlined in this paper, with a focus on ASIC (Application Specific IC) and Gate Array. The impact of the presently evolving BICMOS technology on VLSI is discussed, especially in light of CMOS at low temperatures.

Packaging technology will play a major role on future VLSI chip technology and design. It will be one of the key technical items on product competitiveness. Thin film packages - preferably on silicon - for economic reasons will probably break the trend to ever increasing chip sizes. Brickwall packaged VLSI chips connected via extremely wide buses to memory chips on a common carrier, result in high processor performance at lowest cost. Cooled down to liquid nitrogen temperatures (LNT) by means of a cold plate, these (multi-) processors on a single substrate will attack the performance range of bipolar systems at a fraction of their cost.

1. INTRODUCTION

Will CMOS maintain its leadership position in VLSI technology, or will BICMOS or even GaAs be the choice of the future leading edge VLSI components? This question is rather easily to be answered with regard to GaAs. Despite obvious progress in materials, process and circuit development, GaAs is still suffering from its long infancy. Breakthroughs in high uniformity material and improved surface processing allows to produce chips up to a very few thousands of gates. Despite advantages in logic circuit speed over conventional state of the art CMOS, the need for additional time consuming chip crossings - because of the >10x lower chip circuit count - reduces the performance advantage on a product level. Finally, the still very high production cost will prevent GaAs to be the winner in the VLSI arena within the next 5 years.

The future potential of Bipolar and BICMOS versus CMOS has to be discussed considering and including the appropriate packaging technologies. So far packaging has been a more or less minor support function for VLSI chips, developed from bipolar packages, designed to support high DC currents. In the future, the first level packaging (module) for CMOS VLSI chips - asking for extremely high AC currents in the range of 10A/nS - has to be viewed as an integral part of the VLSI chips, with significant impact on VLSI chip development and chip design concepts. Performance and even more cost of a VLSI product will be influenced severely by the right and optimized packaging technology. This is enforced when a LNT (Liquid Nitrogen Temperature) operation of CMOS is considered, with some high requirements on packaging technology and a 2x performance improvement capability over room temperature operation.

The die size trend of VLSI chips is still increasing according to Fig. 6. However, for economical reasons and electro physical reasons /2/, this trend is unlikely to be continued. As outlined in section 6, the development of CMOS VLSI optimized packaging technologies allow to keep the chip sizes close to constant, without impact on processor performance, and even better packaged density at lower cost.

2.0 CMOS TECHNOLOGY

Despite ongoing discussions on other technologies to take over the leadership in the IC market, the full CMOS technology continues to extend its market share in all major VLSI applications as DRAMS, ASICs and Gate Arrays (see Fig. 1).

Fig. 1 IC Market Trends

The CMOS process technology is driven by the DRAMS with regard to photo lithography and minimum channel length (0.5um for the 16Mb DRAMS). A major push on the wiring technology for ASICs is closing the gap between the achievable circuit density in silicon and the wiring capability of VLSI chips. The leading logic chips utilize 3 layers of metal for interconnections at pitches of 2.6/3.0/5.2 um. The minimum gate length of leading edge ASICs is 0.7 to 0.8um, about one year behind the leading DRAMS.

Because of the longer chip development cycle the more advanced microprocessor technologies are still at 1.0um-drawn CMOS process, with the majority being implemented in a 1.5um technology. The increasing gap in silicon technology between DRAMS and ASICs, and the more advanced wiring technology of ASICs and Gate Arrays, might indicate a change in the future technology driver role from DRAMS to ASICs with

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complex memory macros embedded.

For the advanced VLSI chip applications there is an important trend to be reported. The average 2x improvement in key technological parameters from 1987 to 1989 is surpassed by a microprocessor performance boost of 3x and more in the same time frame. This was achieved by novel architectural implementations, fully utilizing the CMOS VLSI advantages in chip density. Just to mention the key areas:

- deeper pipelining
- separate data and instruction buses
- on-chip parallel processing

This leads to a high performance microprocessor /S/ operating with 0.35 cycles per instruction, or better now with 3 instructions per cycle! This clearly indicates processor performance in the coming years is not driven mainly by technology enhancements as in the past, but due to an "economically induced" flattening of the technology scaling curve, system developers focusing more on architectural optimization will take the lead. For many system designs there is an unexploited performance potential, which is a multiple of the expected performance improvements by pushing a given technology to the ultimate limits.

Within the last years a lack of CMOS VLSI optimized packages, resulting in long off-chip signal delays, forced the development of chips with ever increasing die size. To still achieve reasonable yields, the investments for IC manufacturing facilities will approach 400MM in the early 1990s to meet the stringent requirements on contamination or defect density respectively. If the die sizes are continuing to be increased at the same slope as presently, higher cost on a per circuit level will be noticed for the larger VLSI chips if no redundancy schemes are introduced to compensate for the lower yield.

This yield problem can be solved for the RAM chips by means of the well known redundancy schemes, without a major overhead in chip area. The situation for the logic VLSI chips, however, is more difficult. Because of the lower structurization, a logic redundancy scheme for VLSI logic chips can only be realized with a significant overhead of more than 10% of the total logic for redundant circuits and the associated controls. That means, to achieve an acceptable yield for a 20x20 sqmm ASIC dice, the size has to be increased to 30x30 sqmm to support the redundancy features. This results in lower performance due to longer average wire length on chip, intensified by higher line resistance of narrower wiring lines of future technologies.

A thin film package as described in section 6, gives an option to break the trend of increasing dice sizes - at rising cost per circuit - without negative impact on performance, at a close to 2x better packaged density and lower cost due to smaller chips with less complex chip wiring technology.

3.0 LNT (LIQUID NITROGEN TEMPERATURE) CMOS

A very attractive way for future CMOS VLSI performance enhancements of CMOS processors could turn out to be the operation at low temperatures. A 2x performance improvement is realistic for 0.8 μm technologies. The device speed enhancement is primarily a result of the better electron mobility (a detailed description of CMOS operated at low temperatures is given in J.Wilczynski's paper at the same conference). Despite reduced speed advantage at shorter PET device channels (lower voltage because of hot electron effects), together with the 6x lower resistance of the chip routing at LNT (Liquid Nitrogen Temperature), a performance boost of close to 2x seems to be achievable for 0.5 μm CMOS VLSI chips, without major changes in process. Future CMOS processes and modified circuits, optimized for LNT operation, should give more than a double performance over room temperature operation.

Certainly the LNT operation does not come for free. Cryogenic equipment is required for cooling. The cost of the cryogenic equipment is on a falling slope because of higher volumes for low temperature superconduction applications. The attractive potential of the cryogenic market enabled high efforts in research and development, resulting in smaller and less expensive cooling equipment.

The additional cost - in the range of a few thousand dollars today - for a LNT CMOS based computer is not acceptable for a low performance processor of less than 10 MIPS. But a high performance processor of 50 MIPS and more, even better as parallel operating processors on a single, silicon based carrier (see section 6), attached to a cold plate, would provide extremely low $/MIPS figures for the LNT performance gain.

Other positive side-effects of LNT CMOS are DRAMS operating as static RAMs, keeping the information for up to one week, as a result of lower leakage currents. Furthermore, chip reliability is also significantly better than at room temperature operation.

Last but not least, low temperature CMOS operation already provides the environment for future VLSI chips with superconducting wiring, thus promising a smooth transfer to this strategic technology as soon as it becomes available and profitable. By the way, the euphoria on superconduction potential for VLSI chips, partially expressed in publications, is brought back to earth when it is realized, that the superconduction effect on performance enhancement would be only 20% - 30% if it would be applied today. The remaining 70% - 80% improvement results purely from the low temperature operation effects (higher electron mobility,
lower line resistance, etc.) which are proposed to be utilized today.

There are signs for Japanese companies working on low-temperature CMOS. The fact they don't talk about it at conferences - and instead sell BICMOS, which gives questionable strategic value for VLSI (see section 4) - should be considered another reason for US and European companies to put more emphasis on low-temperature CMOS.

4.0 BICMOS THE FUTURE VLSI TECHNOLOGY?

When the increase of papers from the ISSCC '88 to '89 should be an indication of the future VLSI technology, BICMOS would be the winner. What was (is) the reason for BICMOS being developed, and what is the strategic potential of that technology? An answer is tried to be given in the following.

The initial application of BICMOS was in the chip I/O's to provide better driving capability. Then it was used in the SRAM periphery in sensing and word/bitline driving to speed up access time. Another application is specials with digital and analog function mixes on a chip. All these "niche" applications make sense and will probably be needed also in the future.

The question to be discussed here is what and why made BICMOS a lot of VLSI developers euphoric about future mainstream VLSI applications. First a more emotional argument should be considered. BICMOS primarily is pushed by companies being involved in bipolar technologies in the past. Since bipolar technology, for reasons outlined in section 5, lost more and more ground in the medium performance and even lower high-performance market, they might be motivated to participate with bipolar technology/development in the most attractive market.

The BICMOS 3-way circuit presented by Hitachi at the ISSCC '89 now consists of 16 (!) devices. The euphorically welcomed simple Hitachi BICMOS circuit of the '88 ISSCC had - expectedly - problems with cross-over currents. Therefore, if a BICMOS circuit is compared with a leading edge CMOS implementation of the same process groundrules, there is hardly a factor of two speed advantage on a circuit level (Fig. 3). The existing advantage on a circuit level does not count - a typical suboptimization! - the performance advantage on a product level only counts.

Thus a fast logic BICMOS circuit strategically is driving a longer RC line with even higher resistance in the future due to shrinking dimensions, compared to...
a faster CMOS circuit at low temperature operation, driving a shorter connection, where the resistance is further reduced to about 15% because of low temperature effects on the metal layers.

All key strategic trends of VLSI are not in favour of BICMOS. For high performance applications low temperature full CMOS will provide a 2x faster logic circuit and RAM, connected via low ohmic wiring - or even superconducting wires - should be the winner for the future VLSI ASICs and microprocessors. The 2x market share as projected for 1992 in Figure 1 is primarily based on SRAMS and digital/analog specials.

5.0 BIPOLAR TECHNOLOGY

The bipolar VLSI chips are still suffering very high power dissipation. An ECL VLSI chip consuming 40W has been presented /7, 4/ claiming 50K gates. A critical view on this claim shows an "inflation" of gates. The count seems to be similar "unfair" as the CMOS ASIC manufacturer claiming for huge numbers of gates, whereas 70% ROM/RAM and 30% logic transistors on a chip are summarized and divided by 4, thus giving equivalent gates. Since no delay figures are given, the power-delay product cannot be calculated. From other papers CMOS still has a 3 to 10x advantage over bipolar implementation. On a system level the performance advantage of bipolar technology is reduced as a result of additional signal chip crossings.

Because of economic reasons it is unlikely bipolar will play the major role in future VLSI technologies. The additional cost for packaging, cooling and power supplies will prevent bipolar VLSI to be competitive with CMOS or BICMOS. For high-end processors - where cost plays a minor role - and for analog/digital high speed special applications, the bipolar IC technology merges CAD of VLSI chips and carrier, thus providing an optimized top/down physical design for chips and carrier. No big investments are necessary for manufacturing of such a package, because an "old" CMOS facility can be used!

The wirability per layer is about one order of magnitude improved compared to standard packages. A novel design system with an additional hierarchy step merges CAD of VLSI chips and carrier, thus providing an optimized top/down physical design for chips and carrier. This enhanced physical design concept is key for minimum connection length of signals between chips. The timing critical signal lines on module are reduced to a few millimeters. The short length together with the thin film characteristics - which are similar to on-chip connections - allow to drive chip boundary crossing signals from chip internal circuit to chip internal circuit, resulting in very high speed crossing signals in the range of 1 ns to 2 ns, because no intrinsic delay of driver and receiver has to be accounted for.

The electrical characteristics for a silicon based optimized thin film package are improved by about 2 orders of magnitude in the most important parameter "effective inductance". Therefore, fast and simultaneously switching circuits/drivers are no problem anymore.

The drastically increased number of pads on the VLSI chips contribute to the reduced inductance, improving thermal resistance, and providing a high number of signal I/O's. Another side effect is the off-loading of a major portion of the on-chip power distribution, resulting in smaller and/or denser VLSI chips. Interestingly, the cost reduction of the VLSI chips roughly compensates the cost of the substrate!

The ability to package many fully tested VLSI chips close together gives a 2x better packaged density than for very large chips with the logic redundancy schemes required for yield reasons. Thus, economically, above described package should be a better solution for "wafer scale" integration, particularly with respect to the silicon groundrules approaching critical dimensions in the range of 0.3 um /2/.

Fig. 5 Thin Film Package Schematic
due to novel architectural approaches.

The gap between silicon device density and wiring capability is being reduced (closed) by 3 and more connection layers at aggressive pitches. For economical and physical reasons the still vivid trend to ever increasing logic chip sizes is very likely to be broken in the future.

This potential trend is supported by novel CMOS VLSI optimized thin film packages. It allows to achieve high dense, high performance processors at low cost, without the need for ever increasing chip sizes in the future.

BICMOS was critically discussed and the concerns were described on why this technology probably is not a strategic solution for VLSI logic chips, compared to a full CMOS implementation with the option of low temperature operation for high performance.

Generally, the trend of CMOS to dominate the IC market within the foreseeable future is obvious. BICMOS, Bipolar and GaAs very probably will not successfully attack the CMOS mainstream VLSI leadership within the next five years, for reasons described in this paper.

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