A RATE ADAPTATION GATEWAY TO THE ISDN

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A Multi Standard Rate Adapter coprocessor chip, designed for use in Integrated Services Digital Network (ISDN) terminal adapters and U-interface Modems, is presented. It provides a compact, low power protocol convertor to connect asynchronous (up to 19200 bit/s) and synchronous (up to 64 kbit/s) Data Terminal Equipment with any digital 64 kbit/s network.

INTRODUCTION

A Terminal Adapter provides a connection of any data terminal to a digital network. The connection to the ISDN is established through an S-interface or a U-interface circuit [1], [figure 1]. It allows the interworking of data terminals via the Integrated Services Digital Network (ISDN) as an alternative to the use of voice band modems via telephone networks.

A universal terminal adapter is a key building block in ISDN as current data terminals are using many different signalling standards, electrical interfaces, data formats and bit rates. At the network interface a wide range of transmission schemes are used including subchannel multiplexing.

Currently available terminal adapters based on standard components generally implement only a single rate adaption standard for the network side, and a specific protocol at the terminal side. They are based on standard microprocessors or programmable signal processors implementing a restricted set of functions.

A more universal adapter design based on standard commercial components would lead to a large amount of memory and glue logic. The use of digital signal processor or fast RISC machines provides a non-optimal solution in terms of volume, power and cost.

KEY FEATURES OF THE MULTI STANDARD RATE ADAPTER

The new Multi Standard Rate Adaption coprocessor represents a new quantum in data communication technology. It allows the design of a next generation universal terminal adapter with the following advanced features:

- minimal number of external components,
- reduced power consumption allowing remote feeding,
- compatibility with most synchronous and asynchronous standards,
- multiple rate adaption schemes,
- compact and efficient application software,
- built-in selftest,
- modular design for evolutionary capabilities.

In contrast to existing solutions, the new chip supports both single and multi-channel applications. In single channel applications, a complete system can be implemented using only the rate adapter chip and an 8-bit microcontroller with RAM and ROM. In multi-channel applications up to 256 Rate Adapters can be connected to one PCM highway without any additional hardware. Statistical subchannel multiplexing compliant with CCITT recommendations G.703 and 1.460 is easily realized due to the integrated programmable bus adapter and a flexible bandwidth assignment.

The power consumption of the rate adapter is only 80 mW whereas current designs based on digital signal processors require more than one watt. This allows remote feeding of the terminal adapter.

At the terminal side the rate adapter supports most synchronous and asynchronous data formats (table 1) and signalling protocols of the CCITT V and X series. In addition, synchronous services with network independent clocks are also supported.

Various ISDN rate adaption schemes can be selected under software control. ECMA 102, X.30, X.31, DMI modes 0 to 3, or any other byte synchronous or HDLC based data protocol are supported within the rate adapter architecture.

As powerful coprocessor, the rate adapter only requires a simple 8-bit microcontroller, with limited program and data storage. Bit or byte manipulations of the protocol layer 1 are handled entirely by the rate adapter, as well as part of the layer 2 functions. Protocols without layer 3 (e.g. ECMA102) can be handled without intervention of the controller. Layer 3 data handling can be performed with the on-chip Direct Memory Access (DMA) circuitry. For microcontrollers lacking DMA the interrupt overhead for optional data handling is minimal through the use of internal FIFO's.
A selftest mode based on an on-chip 511 bit pattern pseudo random transceiver and programmable test loops supports component and system tests.

The modular design of the rate adapter chip supports future evolution. The design approach is based on a library of modules and provides the appropriate flexibility requested by the fast evolving ISDN network.

**RATE ADAPTER ARCHITECTURE**

The chip has three main ports: the terminal, the network and the microprocessor port (figure 2). Normal data transfer between terminal and network is performed without intervention of the microprocessor host. The device also allows independent communication of the microcontroller with both the terminal and a remote control unit.

![Figure 2: Rate Adapter Architecture](image)

The low speed terminal port performs a universal synchronous and asynchronous transceiver function, which supports symbol, byte or bit oriented data protocols and multiple selectable clock sources.

The microprocessor port is used for initialization, call and configuration set up, end-to-end flow control, and optional data transfers with network and terminal. Signalling events are handled via interrupts. Data transfers on the microprocessor port run through FIFOs with interrupts or use built-in Direct Memory Access.

At the high speed network port all supported rate adaption schemes are performed in the programmable framing units. Data flow control of transmit and receive paths is based on a 16-word circular buffer.

The baudrate generator derives the appropriate clocks from the selected clock source. If the local oscillator is selected, the resulting clock signal is locked to the network synchronization pulse by a Digital Phase Locked Loop (DPLL) circuit (figure 3). In Network Independent clock mode, the Synchronous Clock Adjust (SCA) information is transferred through the network to the remote side to reconstruct a clock from the network reference (figure 3).

**RESULTS**

The new rate adapter was designed in a 2 micron, double metal CMOS technology. The 50k transistor device dissipates 80 mW in worst case conditions. The total chip area is 6.8 mm x 7.3 mm (figure 4).

![Figure 3: Baudrate Generator Architecture](image)

**APPLICATIONS**

The Rate Adapter chip is a key building block in a new 144 Kbit/s U-Modem (figure 5). Connecting Rate Adapters in parallel to a single chip U-Interface Circuit allows time division multiplexing of up to 16 data terminals onto one full duplex 2-wire 144 Kbit/s link.

![Figure 5: The 144Kbit/s U-Interface Modem](image)

The transceiver chip (UIC) combines all functions that are related to the transmission over the twisted pair. It is connected to a number of rate adapter chips (MSRA), each interfacing with a different data terminal or application. In the basic configuration (2 rate adapter chips) each data connection has a 64 kbit capacity. Using more rate adapter chips (up to 16) is possible through subrate channel multiplexing, allowing a minimum bandwidth of 8 kbit per data connection. System configuration and communication setup are organized by a microprocessor host. Clock and framing information are supplied externally (master mode) or extracted from the receive signal (slave mode). As a result, this system provides low cost access to the ISDN for existing Terminal Equipment.

The rate adapter is a major asset for Terminal Adapter (TA) assembly allowing a simple and cost effective protocol convertor for a wide variety of terminal equipment.

**CONCLUSION**

A new Multi Standard Rate Adapter chip was developed in a 2 micron CMOS technology using a hierarchical design methodology.

The chip provides a compact, cost and power efficient solution for universal terminal adapter design. The Rate Adapter is the cornerstone of a 144 Kbit/s U-Interface modem and a major break-through for the next generation Multi Standard Terminal Adapter.
REFERENCES


Figure 4: Microphotograph of the chip

<table>
<thead>
<tr>
<th>Internal Baudrates</th>
<th>75, 150, 300, ... to 19200 bits/s 1800, 3600, ... to 14400 48000, 56000, 64000 (synchronous only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Format</td>
<td>Asynchronous, synchronous or HDLC 7 or 8 bits per symbol \</td>
</tr>
<tr>
<td>Network Rate Adaption Methods</td>
<td>ECMA 102 or X.30, X.31 DMI modes 0 to 3, HDLC or LAP-B byte synchronous protocols [S1S, DTRD] \</td>
</tr>
</tbody>
</table>

Table 1. Terminal Interface standards and available Rate Adaption schemes.