VLSI CHIPS SUPPORTING PARALLEL BUS INTERFACING AND BUS MANAGEMENT
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Abstract
Several parallel backplane busses have been standardized in the last years each having different bus structures. A number of VLSI interface chips are now available, especially for the widespread VMEbus, each representing different levels and types of functionality. This paper presents an overview of their features.

Bus Characteristics
Busses are commonly defined as data highways connecting a set of digital system elements. The bus is the backbone and plays a vital role in the efficiency, modularity, reliability, and the range of applications and costs of such systems. To interconnect data processing, data storage, and peripheral control devices in a closely coupled hardware configuration parallel backplane busses have got special importance.

Communication between bus participants requires exact keeping of specified conditions. These conditions refer to the logic interfacing (the data transfer protocol) as well as the electrical and mechanical characteristics (drivers, receivers, connectors, board and crate size). For these conditions as well as for realizaiton of parallel busses very different alternatives are existing.

On the one hand there are manufacturer specific computer busses (BI from Digital Equipment Corp., Micro Channel from IBM, etc), on the other hand the application of computing systems in the various domains of process control and data processing claims an exact tailor-making to the specific problems. The solution are open system busses of various manufacturers may be connected together forming powerful systems.

Well known standardized open system parallel backplane busses with 32-bit architecture are:
- VMEbus IEEE 1014
- Multibus II IEEE 1296
- Futurebus IEEE 896
- Fastbus IEEE 896

According to their specifications these busses differ in various items:
- Number of signal lines (connectors, pins)
- Multiplexed / Nonmultiplexed address and data path
- Byte orientation and justification
- Synchronous / Asynchronous data transfers
- Interrupt handling
- Central / Distributed arbitration
- Priorities by request level / by slot position
- Shared-memory / Message passing for interprocessor communication
- Means for self-configuration (geographical addresses, broadcast)
- Electrical issues (logic signals, bus terminations, power supply)

Basic Bus Structures
Bus specifications define bus signal lines, signal transceivers and functional modules (Fig. 1).

Functional modules are defined to handle the bus protocol. They represent the link between the implementation dependent application area and the standardized communication path via the backplane. Typical functions are Data Transfer Handler (e.g. Master, Slave), Bus Arbiter, Bus Requester, Interrupt Requester / Handler, Message Passing Controller, System Controller etc.

Signal transceivers are the line drivers and receivers which take into account the characteristics of the backplane: its line impedance, propagation time, termination values, etc. The number of signal lines and their specific function differ from bus to bus dependent on the bus architecture.

The 32-bit multimaster / multiprocessor busses necessitate a high complex interface busy. Bus interfaces implemented with discrete ICs or PLDs can take up to 50% of the pc-board real estate available. The trend to place more functions on a single board increases the need for high integrated interface chips.

Bus Interface Chips
Now after bus specifications have become standards, a number of VLSI interface chips for 32-bit backplane busses are readily available. At least nine VMEbus ASICs (Application Specific Integrated Circuits) are on the market or have been announced (Table 1), each representing different types of functionality. Most of the manufacturers offer a single-chip solution. These chips equip a board as full-featured system controller and master/slave unit with interrupt requester and handler. Unused functions can be disabled. Some manufacturers split the master/slave function into two chips, saving board real estate and costs when building master only or slave only boards.

Most of the chips include features, which are not standardized, but do not violate the bus specifications, in order to increase the efficiency of the bus system (e.g. message passing). Those extra facilities can only be used in systems containing the specific chip on all participating boards. This is a serious disadvantage for implementation of application-specific systems by other manufacturers [1,2].

Besides the ASIC solution above there are some LSI (Large Scale Integration) chips and PLDs (Programmable Logic Devices) supporting single functions as system controller, master/slave data transfer controller, interrupter or interrupt handler (e.g. VMEbus controller circuits from Valvo / Signetics [3], PLD-based VME interface controller from Advanced Micro Devices [4]).

In the Multibus II world only one ASIC exists, which already provides a nearly universal functionality: the Message Passing Coprocessor chip (MPC), designed by Intel and first manufactured by VLSI Technology, now available from both companies.

The advanced Futurebus, just having been standardized by IEEE, is not yet supported to any significant degree by board manufacturers, and no bus interface chip exists. But Futurebus has solved, for the first time, the fundamental problems of driving a densely populated backplane. According to the requirements of the Futurebus specification, National Semiconductor has developed its Bus Transceiver chip...
Logic (DS38xx Series). These transceivers include low output capacitance drivers to minimize the bus loading, and receivers with precision thresholds for maximum noise immunity.

Examples of VMEbus Interface Chips

The VMElchip MVME 6000, developed by Motorola, provides all functions required to interface 68020/68030 microprocessors to the VMEbus (5). The chip is composed of nine functional blocks. These are master, slave, requester, arbiter, interrupter, timer, local control and status registers, and the global control and status registers. All functions are programmable by software. Unused functions can be disabled. In addition to the VMEbus-defined functions, the chip includes the following major capabilities to support multiprocessor architecture:

- Local control and status registers - to control and configure the operation of the chip and to provide status information that allows software to monitor its interaction with the environment (only accessible to the local processor).

- Global control and status registers - to support the operation of the board in a multiprocessor environment. It provides facilities that allow other CPU boards to interrupt the local processor, to communicate with it, to monitor its operational status and to disable it. The GCSR contains four location monitors which allow a single CPU to broadcast a signal to up to 14 other CPU boards.

- Write posting - controls the latching of outgoing address and data information, provides an early acknowledge to the local microprocessor and completes the VMEbus write cycle on its own.

- Cache Fill - executes a 4-byte VMEbus read cycle regardless of the amount of data that the local microprocessor requests during a read cycle that accesses a D32 slave.

The Force FGA-002 (Fig. 2) is the biggest Gate Array of all VMEbus ASICs (20,000 gates, 290 pins). It includes a 32-bit DMA controller, which can send bursts of data across the bus at 30 Mbytes/s. During a DMA transfer the local CPU has full access to local memory, EPROM and I/O controllers. Communication and synchronization between CPUs in multiprocessor systems is supported by 16 location monitors.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Type</th>
<th>Chip</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motorola</td>
<td>MVME 6000</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / System Controller / Global Control and Status Register Set</td>
</tr>
<tr>
<td>Motorola</td>
<td>MVME 2400</td>
<td>PGA</td>
<td>Bus protocol for VME Subsystem Bus (VSB)</td>
</tr>
<tr>
<td>Force Computers</td>
<td>FGA-002</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / Arbiter / Message Broadcast / Location Monitors / DMA support / VSB support</td>
</tr>
<tr>
<td>VME Consortium manuf. by VTC Inc.</td>
<td>VIC 068</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / System Controller / Location Monitors / Interprocessor Communication Register / DMA support / TAS, CAS support / connected directly to VMEbus</td>
</tr>
<tr>
<td>Electronic Modular Systems Inc.</td>
<td>EMychip</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / System Controller / DMA support / 4 Location Monitors / TAS, CAS support</td>
</tr>
<tr>
<td>VLSI Inc.</td>
<td>CDG (Controller) DGA (Data Handler)</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / System Controller / Location Monitors / TAS, CAS support / DMA support / Self-conf. support</td>
</tr>
<tr>
<td>DV - 4 Systems Inc.</td>
<td>DY-4401 (ACC) DY-4402 (DARF)</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / System Controller / Location Monitor / DMA support / ACC connected directly to VMEbus</td>
</tr>
<tr>
<td>SBE Inc.</td>
<td>VBIC, VSAM</td>
<td>PGA</td>
<td>Master / Slave / Interrupter / Interrupt Handler / System Controller / 1 Location Monitor / 16-bit Mailbox</td>
</tr>
<tr>
<td>Cipriano Inc.</td>
<td>PSJ</td>
<td>PLCC</td>
<td>Slave only / A16, A24, A32 addressing / Interrupter / programmable AM code / address pipelining</td>
</tr>
<tr>
<td>Performance Technology Inc.</td>
<td>PT-VSI</td>
<td>PLCC</td>
<td>Slave only / A24, A32 addressing / Interrupter / 16 Mailboxes / programmable AM code / connected directly to VMEbus</td>
</tr>
<tr>
<td>Mitic Inc.</td>
<td>VME 1000A</td>
<td>DIL</td>
<td>System Controller with 4-level Arbiter, Bus Timer, System Reset, connected directly to VMEbus</td>
</tr>
</tbody>
</table>

Package Types: PGA - Pin Grid Array / PLCC - Plastic Leaded Chip Carrier / DIL - Dual In-line

Table 1: VLSI Chips for VMEbus

Fig. 2: Block Diagram of the VMEbus Chip Force FGA-002
Another important feature is the Force Message Broadcast concept (FMB). This programmable protocol allows to pass one-byte broadcast messages in only one bus write cycle to any processor or intelligent controller board, that supports this principle. This function is provided by two independent FIFO channels allowing prioritizing of messages. Additional features of the chip are:
- management functions for dual-ported memory,
- complete, software-controlled address of local CPU and VMEbus accesses to the dual-ported memory with the ability to define write-protected areas,
- four individual programmable 8-bit timers.

The chip does not include a VMEbus interrupter, and provides a single-level arbiter only [6].

The VIC 068 chip, manufactured by VTC Inc., is the only VMEbus ASIC that was cooperatively developed by a consortium of more than 20 VME vendors like Plessey Microsystems, Omnilyte Corp., Mizar Inc., Ironics Inc., Heurikon Corp. This chip includes complete system controller and master/slave capability, interrupter and interrupt handler. Additional functions are 4 broadcast and 4 module-specific location monitors, 8 interprocessor communication registers as well as programmable delays for some control signals (DSACK and DTACK), address pipe-line option, master/slave write-posting option, TAS / CAS / CAS2 instruction support for 68020 processors and interleaved block transfers for DMA. The chip connects directly to the VMEbus lines.

Dual-chip sets for the VMEbus are offered by VLSI Inc., DY-4 Systems Inc., and SBE Inc. The chips from VLSI Inc. consist of a controller and a data handler PGA, supporting complete VMEbus interface handling, interprocessor mailbox-message passing, implemented by a 1 KByte buffer and FIFO controller, a real-time clock, accessible from both the local bus and the VMEbus, DMA transfers and other features.

The DY-4 System a interface chip set consists of the ACC (Advanced system architecture Control Circuit) and the DARF (Data & Address Register File). The ACC performs typical system control and master functions, and includes a built-in test function and a bus isolation mode. During the test procedure, and upon any failure, the chip disconnects its local board from the system, allowing the rest of the system to continue to function normally. The DARF allows the on-board CPU to access the VMEbus, and offers other masters a window of access into the memory map of the local CPU. The base address and size of the window are controlled by registers inside the DARF. Furthermore the DARF includes a DMA controller and a location monitor. The DY-4 chip set sustains memory-to-memory data transfer at the theoretical limit of the VMEbus of 20 Mbytes.

SBE Inc. offers the VBIC (VMEbus Interface Controller) and the VSAM (VMEbus Slave Address Manager) chips to implement either a full master or a slave interface. The chips combined support local interrupt handling, multiprocessor communication control via a mailbox register and location monitor, and system control functions confined to bus slot 1.

**Multibus II Message Passing Coprocessor**

The message passing protocol has been well defined in the Multibus II specification. The single-chip Message Passing Coprocessor (MPC) from Intel / VLSI Technology Inc. is a highly integrated ASIC device implementing the full message passing protocol as well as the full functions of the Parallel System Bus (PSB) such as arbitration, transfer and exception cycle protocols (Fig. 3). The MPC is a functional superset of the former 2-chip interface set, the BAC (Bus Arbitration Controller) and the MIC (Message Interrupt Controller).

The Multibus II architecture defines a message passing space to provide high performance interprocessor communication mechanism for multiprocessor systems. One of the key functions of the MPC is to support the message space interface by offloading the local CPU from interprocessor communication tasks, whereby the local bus activities are decoupled from the PSB (Parallel System Bus) activities. MPC-based boards can sustain a 32-Mbyte/s data transfer rate. The MPC is not designed to operate directly in a shared-memory environment, but it simplifies the implementation of that function. Only some circuitry has to be added to a MPC-based board to perform shared-memory access via the parallel bus to nonintelligent boards. Additionally, the MPC chip supports CSM (Central Service Module) functions, such as system clock, reset-sequence generation, card-slot and arbitration ID initialization, and time-out signal generation. Some external logic has to be used to implement some CSM features, but the MPC couples the CSM circuitry to the bus. Since there is only one Multibus II interface chip on the market, every board manufacturer implements a nearly identical interface resulting in high system compatibility [7].

**References**


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**Fig. 3: Block Diagram of the Multibus II Message Passing Coprocessor**