FIELD EXPERIENCE WITH CUSTOM
LSI CHIP SET FOR ISDN

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Introduction

ISDN can be characterized by three main functions. First is end to end digital connectivity. Second is powerful signalling at subscriber/network interface (D channel protocol). Third is support for packet switching. For these requirements Standard Components were not available on the market in time.

The SEL and BELL groups of Alcatel have developed an ISDN chip set which will ensure a cost effective and reliable implementation of ISDN for System 12 exchanges, terminal adapters, terminals and subsets. The custom LSI chip set is an improvement on those already used in an ISDN Pilot Project for "Deutsche Bundespost" which gave good results on maintainability, reliability and availability.

An effective, modular and flexible ISDN chip set concept has been developed using functional partitioning at board and integrated circuit level based on the distributed architecture of System 12. As System 12 can handle both speech and data connection with equal ease, the only enhancements needed to provide ISDN services are new peripheral modules for packet oriented services.

ISDN LSI Chip Set

The ISDN chip set consists of five custom LSI's: UIC, ILC, SIC, OBCI and DTIC. (Key characteristics see table 1.)

The circuits operate at Layer 1 and Layer 2 of the OSI communication network model using HDLC (high level Data link control) protocols in accordance with CCITT X.25 and CCITT No. 7 (2, 3).

2-wire UIC (U interface circuit)

A key factor in the economics and performance of ISDN is the choice of a transmission method for use on existing 2-wire telephone lines which suffer from noise. The transmission range and reliability achieved by the UIC are a result of careful choice of line code and synchronization method. The 4B/3T line code is used.

The UIC is a Layer 1, full duplex interface circuit for 2 wire, 144 kbit/s basic access.

- 2- to 4-wire hybrid based on echo cancellation for line length up to 8 km
- Maximum allowed bit error rate < 10(-7) caused by crosstalk and noise.

- V' Interface

- Activation/deactivation after a maximum setup time < 150 ms, power consumption 5 mW in power down

- Word and frame synchronization using a digital correlation phase locked loop.

The UIC is divided into three functional sections: analog front-end, digital signal processors and subscriber exchange interface.

The analog front-end is the interface between the digital part and the outside world.

Highly sophisticated circuitry is implemented:

- ROM based transmit filter
- Pulse density modulator
- Second order low pass filter
- Sigma-delta modulator
- Two-dimensional systolic array
- Signal processors are implemented to support the echo canceller, equalizer, gain control

ILC (ISDN link controller) for layer 2 functions

The ILC performs multiplexing and demultiplexing for B and D channels with the following key features.

- V' interface compatibility
- 256 kbit/s ILC-SIC interface
- Two HDLC formatters per receive and transmit port (programmable for 64 kbit/s or 16 kbit/s depending on whether packet data is sent on the B or D channel).
- 8- or 16-bit microprocessor interface
- On-board direct memory access controller for packet transfer.
- Two serial 64 kbit/s receive/transmit codec interfaces.
- Programmable for basic access, primary rate access, or CCITT No 7 common channel signalling applications.

4-wire SIC (S interface circuit)

The SIC has access to the 8- and D-channel via the standardized So interface including master/slave functions.
Activation and deactivation is supported as well as incoming and outgoing calls.

**DTIC (digital trunk interface circuit)**

The DTIC is the interface between various 2048 kbit/s digital trunk formats and the switching network. A CRC4 check is implemented.

**OBCI (on-board controller interface)**

The OBCI is an intelligent CLSI which provides a control and transmission interface between the network terminals (analog and digital) and the terminal control element.

One of the tasks is to switch any incoming channel to any outgoing channel. OBCI can set up 72 paths. Also a free channel search mechanism is implemented.

<table>
<thead>
<tr>
<th>Table 1 - Key characteristics of the ISDN chipset</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Transistor count</td>
</tr>
<tr>
<td>Die size (mm²)</td>
</tr>
<tr>
<td>Number of pins</td>
</tr>
<tr>
<td>Clock rate (MHz)</td>
</tr>
<tr>
<td>Power (mW)</td>
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</table>

*) power-down mode

**Reliability, Design, Qualification**

The system dependability is described amongst other characteristics the service availability. It is a measure of the probability that digital trunks or subscriberlines are able to access the exchange successfully and that the connection is handled properly.

A > 0.99977, or (unavailability < 2 h/year)

A complete reliability calculation was carried out for the exchange including hardware and software. This detailed calculation is required by the customer, and includes printed board assembly failure rates, failure criteria, maintenance support, environmental conditions, reliability analysis based on block diagram, redundancy, reliability model and components failure rates. The prediction is based on the MIL Handbook 217, inhouse failure rate data bank, and qualification testing.

<table>
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<td>The ISDN core functions are used in both public and private ISDN digital loops. Typical ISDN digital loops with the custom LSI: UIC, ILC, SLC, OBCI and DTIC are illustrated in Figure 1. The terminating equipment is connected via Network Termination (NT) with the ISDN subscriber modul using a data rate of 144 kbit/s. The concentrator (or primary rate access network) is connected to the ISDN trunk modul using a data rate of 2.048 Mbit/s.</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Technology</th>
<th>ILC</th>
<th>OBCI</th>
<th>UIC</th>
<th>SIC</th>
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<tbody>
<tr>
<td>failure rate (10^-9/h)</td>
<td>200</td>
<td>350</td>
<td>250</td>
<td>120</td>
</tr>
<tr>
<td>predicted</td>
<td>70</td>
<td>80</td>
<td>140</td>
<td>70</td>
</tr>
<tr>
<td>“life test”</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40 °C ambient</td>
<td></td>
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</tbody>
</table>

To fulfill these requirements a complete qualification program was executed.
Worst case design

The requirements of the CLSI are specified in detail specification. The design rules used for the chips are fully characterized and agreed between chip designer and supplier. Any change of process will be reported to the designer. This is supervised by the quality inspector of Alcatel.

Characterization of the chip

All chips were fully characterized on automatic test machines. This is a measure of the safeguard. The characterization is done at extreme temperature and electrical parameters. The characterization before and after life test gives a measure of the stability of the chip.

A typical graph is given in Fig. 2

Component Qualification

- functional test
- electrical AC, DC-parameter
- sealing
- transient energy
- mechanical test
- visual inspection
- X-Ray testing of the die attach
- temperature cycling
- temperature shock
- life test 2000 h/125 °C

The failure rate based on our life test results is roughly one half of the values which were used for the reliability calculation.

Board level test

In addition to component qualification, a complete qualification test with the complete printed board assembly was carried out before we started integration testing for the total system.

Component screening

All components were tested with automatic test equipment at 25 °C and at the extreme specified temperature. In addition a "burn in" at 125 °C is carried out to reduce the early failure rate.

Integration and Field experience

Before System 12 was installed in service, valuable information on system behaviour was collected from integration and laboratory testing. Number of events, errors were collected during the complete software life cycle of integrating the software.

No indication was found that the predicted reliability and availability requirements would not be met.

Hardware

The major ISDN functions are implemented in the LSI chip set, but the impact of CLSI hardware reliability is less than 10%.

Conclusion

System test and field experience have shown that the development and quality strategy is correct. The predicted performance reliability and availability were reached. The key to successful ISDN is the high integration of the major function in VLSI technology. As in the past the prediction of the failure rate of CLSI was too pessimistic. This demonstrates the steep learning curve for VLSI chips.

References


(2) Van Iseghem P., Danneels J.M., Rahler M.C., Krüger A., Szeczenyi K. ISDN Components for Public and Private Digital Loops

(3) Szeczenyi K., Zapf F., Implementation of the U Interface Circuit
Figure 1

Typical implementation of the five VLSI circuits with make up the ALCATEL ISDN chip set.

Figure 2

Characterization of Input set up time versus supply voltage