Thin Film Transistors for Addressing LC-Flat Panel Displays

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Abstract

Thin film transistors (TFTs) are exceptionnally qualified for addressing large area LC-displays. The TFT-circuits and the requirements for operating the picture elements in the displays will be described. Further comments focus on the staggered structure of the TFTs and the materials a-Si:H and poly-CdSe used as semiconductors and Ta2O5, SiO2 and SiN for gate isolators.

The electrical data such as mobility and off-current of the TFTs determine the optical performance of the displays characterized by a high contrast and a wide viewing angle.

1. Introduction

Active matrix addressing of liquid crystal displays (LCDs) by thin film transistors (TFTs) [1], [2] represents the most promising technology for addressing large area and high resolution screens in computer applications as well as full color pocket and full size TV-sets or projection displays.

The integration of a TFT in each picture element (pel) as a switch for connecting the appropriate video signal to the selected pel and for blocking the other signals during the remaining frame time provides a 100% duty cycle of the pel. Thus, best values of contrast, viewing angle, gray scales and color capability of the displays can be obtained.

Furthermore, the TFT-technology offers the only possibility for an integration of shift registers and video switches on the same substrate for driving the x- and y-lines of the display.

2. The TFT-matrix and the addressing voltages

Fig 1 shows the circuit diagram of a matrix with m columns and n rows fabricated simultaneously on the main glass substrate, while on the counter glass plate only a non-structured transparent electrode is placed. The layout of a pel is given in fig 2.

The pels are addressed one line at a time by the voltages depicted in fig 3. The polarity of the video-signals Vp must be alternated after each frame time to prevent a DC-biasing of the LC causing electrolytic decomposition.

Fig 1: The TFT-addressed LC-matrix

Fig 2: The layout of a pel

Fig 3: The addressing voltages
3. Requirements of TFTs for addressing pels

Basic values for the following calculations are a refresh time $t_r = 20$ ms corresponding to a frame rate of 50 Hz and a display with $n = 288$ lines ($m = 400$ columns) and a pel capacitance of $C = 0.1 \, \text{pF}$. Under these assumptions the dwell time $t_d$ for addressing one line is $t_d = t_r/n = 69$ $\mu$s. Therefore, the time constant $\tau_{on}$ for charging all pel capacitances $C$ in a line is required to meet $\tau_{on} = R_{on} \times C < 1/10 \times t_d$, where $R_{on}$ represents the on-resistance of the TFT. From that an $R_{on} < 69 \, \text{M} \Omega$ is determined. The time constant $\tau_{off}$ for a negligible discharging of the pel during the non-addressed time $t_r - t_d = t_r$ is $\tau_{off} = R_{off} \times C > 10 \times t_r$, where $R_{off}$ is the resistance of the blocked TFT in parallel to the leakage resistance of the LC. From that requirement follows $R_{off} > 2000 \, \text{GO}$, which can be lowered by a larger $C$-value when an additional storage capacitor in parallel with the LC-cell is built in, as depicted in fig 1 and fig 2.

4. Gate dielectrics and semiconductors for TFTs

4.1 Dielectrics

<table>
<thead>
<tr>
<th>Material</th>
<th>relative Die./ Depos</th>
<th>Const. $\varepsilon_r$</th>
<th>Deposition</th>
<th>special features</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiNx</td>
<td>15-9</td>
<td>PECVD*</td>
<td></td>
<td>mostly used for a-Si-TFTs, deposition in same run as a-Si ensures low trap densities</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>4</td>
<td>PECVD or sputtering</td>
<td></td>
<td>similar characteristics as SiNx</td>
</tr>
<tr>
<td>Ta$_2$O$_5$</td>
<td>22-24</td>
<td>Anodization</td>
<td></td>
<td>high $\varepsilon$ provides high currents, wet anodization provides self healing process</td>
</tr>
<tr>
<td>Ta$_2$O$_5$+SiO$_2$ (or SiNx)</td>
<td>Anodization</td>
<td></td>
<td>medium $\varepsilon$, medium currents, SiO$_2$-semiconductor interface — low trap density</td>
<td></td>
</tr>
</tbody>
</table>

4.2 Semiconductors

<table>
<thead>
<tr>
<th>Mat.</th>
<th>Mobility $\mu$</th>
<th>Deposition</th>
<th>special features</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si:H</td>
<td>0.7</td>
<td>PECVD</td>
<td>mostly used for TFTs in pels; mobility too low for high speed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>shift registers and video switches</td>
</tr>
<tr>
<td>poly-Si</td>
<td>&lt; 80</td>
<td>PECVD</td>
<td>high depos. temperature/recrystallization temp. requires quartz glass substrates</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>compound semiconductor for high current and high frequency applications</td>
</tr>
</tbody>
</table>

*plasma enhanced chemical vapor deposition
5. Structures and manufacturing processes of TFTs

The sequences of layers for TFTs, in two proven versions, one with amorphous Si [3], [4] and the other one with polycrystalline CdSe [5], [6], are outlined. Comparable systems for poly-Si-TFTs are described e.g. in [7].

5.1 a-Si:H-TFTs

A cross section of a TFT with a-Si:H as semiconductor, in which traps are saturated by hydrogen is given in Fig 4. The gate dielectric SiN, the a-Si:H semiconductor, and the P-doped n'-Si-layer are successively deposited by PECVD in one vacuum run. The n-Si-layer, which can be removed selectively from the channel area, guarantees a transition with low resistance from the metallic drain and source contacts to the semiconductor. Instead of the n+-layer also a thin Mg-layer as an interface layer may be used [8].

5.2 Poly-crystalline CdSe-TFTs

The structure of the TFTs and the materials used are shown in Fig 5. The generation of the Ta$_2$O$_5$-gateoxide by anodization [9] ensures a high dielectric covering the gate without applying a mask. Further, the deposition of an additional thin SiO$_2$-layer [10] by sputtering or CVD reduces both the number of pinholes and weak spots as well as the trap density at the oxide-semiconductor interface resulting in a high yield and low drift behavior [8]. The drain and source overlap capacities are minimized by evaporating the contact material in a photoresist mask, which is exposed from the rear side of the substrate using the opaque gate as a self aligned photo mask. The CdSe is evaporated in ultra high vacuum after cleaning the substrate surface by sputtering in the vacuum interlock of the system. Crystallization of the originally amorphous CdSe succeeds in a three step annealing with decreasing temperatures of 350, 300 and 250°C in vacuum, air and again in vacuum.

Fig 6: Drain source current I of a CdSe-TFT versus gate voltage $V_g$ at $V_{ds} = 10$ V

Fig 7: Drain source current I of a CdSe-TFT versus drain source voltage $V_{ds}$ with $V_g$ as a parameter
7. Optical characteristics of TFT addressed displays

As an example for the high optical performance of TFT-addressed displays the measurements of contrast at various viewing angles of a black and white display are depicted in fig 8. In the optimum direction the display exhibits a maximum contrast of 1:48 which only decreases to 1:16 at horizontal viewing from 12 o'clock.

Fig 8: Contrast and viewing angle of a CdSe-TFT-addressed display

8. Present state of the art

Recent developments in the United States [3] and in Japan [4] resulted in direct view displays with full color capability, screen diagonals of 8" and 14" respectively, and more than 10^6 pels addressed by a-Si-TFTs. The efforts with projection displays led to full color TV-projectors [12] with at least half the resolution of CRTs (around 300 000 pels). The 3 basic colors are modulated by 3 separate TN-LC-light valves with integrated x- and y-drivers containing poly-Si-TFTs [7]. The 3 color beams are superimposed by a dichroic mirror prism. The illumination of an 1 x 1,3 m² screen is about 110 lx.

9. Summary

LCDs addressed by TFTs turn out to be a serious challenge to CRTs for applications where low weight and low volume are required. The materials used as gate dielectrics and as semiconductors are SiN and a-Si:H for low current lower speed devices and SiO₂ and poly-Si or Ta₂O₅ and CdSe for higher current high speed applications. Especially the latter ones are also suitable for integrated shift registers and video switches driving the x- and y-lines of the matrices at higher frequencies. Research and development of TFTs focuses on large area and high yield fabrication.

10. Acknowledgements

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11. References

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[10] M. Katayama et al, High Resolution Full-Color LCDs Addressed by Double Layered Gate-Isolator aSi TFTs, SID Digest 88, 310