ABSTRACT

Ferroelectric materials show a spontaneous electrical polarization that can be reversed in sense by an applied external electric field. It should, therefore, be feasible to build a ferroelectric memory device that can store information in digital form.

Early attempts to build such a memory have failed for various reasons, the major one being a lack of a well defined and stable coercive field, which resulted in the eventual loss of data due to half-select pulses applied to unselected cells in the crosspoint array architecture. Fatigue or wear out was also a problem in that the amount of available signal depended upon the number of polarization reversals.

We have been able to overcome these problems by a combination of design innovations and process and materials breakthroughs. We have chosen PZT (lead zirconate titanate) as the basic ferroelectric material and integrated it into a standard CMOS process. PZT has a wide temperature range (-350°C Curie Temperature), low coercive voltage, high specific polarization charge (10-20pC/µm²) and good retention and endurance. The lack of a well defined coercive field was overcome with a DRAM like circuit architecture, which provides for transistor switches in series with each ferroelectric element preventing disturb pulses from affecting the unselected cells.

As a demonstration vehicle, a fully decoded 256 bit nonvolatile ferroelectric Random Access Memory (FRAM™) was developed. Characterization results will be presented. One of the unexpected findings was the extremely fast switching speed inherent in the PZT material, which was found to be of the order of one nanosecond. The high switching speed and the high signal charge, which renders the technology highly scalable, offers the potential to build nonvolatile semiconductor memories with the speed of static RAMs and the density and cost of dynamic RAMs.

I. Introduction

The ferroelectric effect is not a new discovery. As early as 1921 J. Valasek discovered the phenomenon of spontaneous polarization on Rochelle Salt (Na,K,H2O11,5H2O) and used the term "ferroelectric" to emphasize the analogy between the non-linear hysteretic dielectric properties of Rochelle Salt and the magnetic behavior of ferromagnetic iron. Spontaneous polarization means that electrical dipoles in the material align themselves along electrical field lines when an electric field is applied to a specimen and remain in the aligned position even if the field is subsequently removed. Applying the opposite polarity causes the dipoles to switch and align in the opposite direction.

Because ferroelectric materials exhibit at least two stable states that can be switched back and forth, it should be feasible to build a ferroelectric memory device that can store information in digital form. A major attempt was made in the 1950s and 1960s by researchers in several laboratories to build such a nonvolatile memory. At that time ferroelectric technology was considered an attractive alternative to the main stream magnetic core technology. However, most of these attempts were abandoned for a variety of reasons. One of them was the imperfect shape of the Q-V hysteresis loop (as compared to the ferromagnetic analog (Figure 1), which made it difficult to implement a ferroelectric capacitor element in a memory array. The only memory architecture considered at that time was the crosspoint matrix array shown in Figure 2. Because most ferroelectric materials lack a well defined and stable ferroelectric switching threshold voltage (coercive voltage) (see Figure 1), data to a memory is eventually lost due to the half-select pulses applied to unselected cells.

Another obstacle to the creation of a ferroelectric memory in the 1950s and 1960s was the lack of a deposition technique that could achieve high quality deposition films. Early ferroelectric memories employed bulk material that resulted in switching thresholds of tens or hundreds of volts and switching speeds in the range of microseconds to milliseconds rendering the technology incompatible with integrated circuit technology.

A further limitation to practical memory applications was the limited endurance (decreasing signal charge as a function of switching cycles) of most ferroelectric materials. Endurance varies widely and can range from a few cycles to >10⁸ cycles depending on the material chosen and subsequent processing.

The attempts to build a ferroelectric memory had essentially been abandoned in the early 1970s when the industry has taken a different route toward satisfying the need for nonvolatile memories. Volatile semiconductor memories such as dynamic RAMs or static RAMs have effectively replaced magnetic core memories. However, nonvolatility is quite often an important requirement which is accomplished with a DRAM like circuit architecture by writing back-up in the board-or-system levels. However, for many applications nonvolatility on the component level is preferred. Numerous nonvolatile technologies (both semiconductor- and magnetic-) were developed such as ROM, EPROM, EEPROM, MROM, plated wire, bubble technology, etc. The fact that not one, but many different forms of nonvolatile memory components exist today, illustrates clearly that no one single technology can satisfy all the requirements.

There is no doubt that a nonvolatile memory technology that could offer low cost/bit, high speed, good retention, and high endurance and be compatible with standard semiconductor technologies such as CMOS, GaAs, etc. would have tremendous potential and an essentially unlimited market. I would like to show that the ferroelectric technology being developed by RAMtron has the potential to approach this "ideal memory technology." First, the basic technology will be described and then the results will be presented that have been achieved with discrete memory capacitors as well as on a 256 bit nonvolatile Ferroelectric Random Access Memory (FRAM™) that was developed as a demonstration vehicle (FRMs 8101).

II. Ferroelectric Memory Element

There are basically two ways to build a digital memory element employing a ferroelectric thin film dielectric. One approach is to replace the gate insulator of a field effect transistor with a ferroelectric layer. The threshold voltage of such a device will have two distinct values depending on whether the dipoles in the ferroelectric material are oriented up or down. The advantages of this implementation are the inherent amplification built into the device and the unlimited read cycles (the device is only fatigued if new information is written into it). It also offers the potential for a memory with a very high packing density, since only one device per cell is required.

However, this device is very difficult to build reliably. First, in order to obtain low voltage switching, low resistance electrodes are required. This is difficult to achieve, at least for the bottom electrode (ferroelectric-silicon interface) without destroying the transistor characteristics.

Figure 1. Comparison of Magnetic and Ferroelectric Hysteresis

Figure 2. Cross Point Matrix

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Secondly, as shown by J. Schult et al. due to the movement of slow compensation charge through the ferroelectric layer the two distinct threshold voltages corresponding to a high "U" and a logic "1" approach each other with time. Therefore, the information is lost after some time which can be from several seconds to hours or days.

The second implementation is the one adopted by Ramtron, a ferroelectric capacitor as shown in Figure 5a. The device consists of a layer of ferroelectric material sandwiched between two metal electrodes. The device is written by applying a voltage \( V \) which is greater than the coercive voltage of the structure. Under the influence of the electric field, the dipoles are aligned in one direction (up in our example). The device is read by again applying a voltage \( V \) across the device. If the dipoles are oriented in the direction of the electric field a current pulse is generated that corresponds to the charging current of the capacitor. This current is proportional to the linear dielectric constant of the material.

\[ \sqrt{V} \text{ (in V)} = 20 \text{ns} \]

Figure 3a. Ferroelectric Capacitor

If however, the dipoles are oriented in the opposite direction, a larger current pulse is generated that is the result of the charging current of the capacitor and the switching current caused by flipping the dipoles in the opposite direction. A logic "0" or "1" can be detected depending on whether or not the switching current due to the change of dipole orientation is present. In other words, the difference between switched or non-switched charge is the signal charge which is sensed in a fashion similar to DRAMs. Therefore, similar to the operation of a dynamic RAM, reading a ferroelectric capacitor is always destructive and the information has to be written back to the device after every read cycle. In contrast to the ferroelectric field effect transistor, the ferroelectric capacitor is not sensitive to mobile charge movement. The information is preserved even after the device is fully compensated and the voltage across the device has decayed to zero. The alignment of the dipoles is not altered and can be detected by pulsing the device. Figure 3b illustrates the read/write operation of the device where four voltage pulses are applied to the device and the current response is plotted as a function of time. This data was obtained from a capacitor employing PZT (Lead zirconate titanate) as a ferroelectric material.

Several important features are evident from Figure 3b. First, the switching time is very short. The current pulses have decayed to zero in less than 80ns. It will be shown later, that most of the time delay is caused by parasitics and inadequate instrumentation. The inherent switching time of PZT, is of the order of 1ns. Secondly, the signal charge, which is the area between N and D or P and U is large, of the order of 15pC/cm². This renders the technology highly scalable. As will be shown later, in a dynamic RAM implementation, a 1x1x1 ferroelectric capacitor will develop a bit line voltage differential of about 200mV which is well above the detection limit.

III. Ferroelectric Technology Integration

Of the many hundreds or even thousands of known ferroelectric materials, only few are suited for switching applications and can be integrated into a semiconductor technology. To be commercially feasible the ferroelectric material has to have good retention and endurance, adequate dielectric breakdown for substrate layers, a coercive field compatible with five volt operation and a signal charge of at least 5pC/cm². The Curie temperature should be sufficiently above the highest storage temperature and inherent switching speeds should be in the nanosecond range. The deposition technique should be compatible with standard semiconductor processing.

We have chosen PZT (Lead zirconate titanate) as the preferred ferroelectric material. PZT satisfies all of the above requirements.

PZT can be deposited in thin film form in various ways. Methods reported in the literature include Sol-Gel processing, MOD (Metallo-organic decomposition), Chemical Vapor Deposition, and Sputtering.

We have chosen RF Magnetron Sputtering from a single ceramic target as the preferred method of deposition mainly because it is compatible with standard CMOS processing and offers excellent control of film thickness, stoichiometry and adhesion to the electrodes.

Ferroelectric processing using PZT as the base material is a true add-on technology to standard semiconductor processes. Figure 4 shows how it is integrated into a standard CMOS process. The bottom electrode, the PZT layer and the top electrode are placed on top of the underlying CMOS circuitry before Source/Drain/Gate contacts are cut and before the interconnect (e.g. Aluminum) technology is applied. From one to three additional masking operations are required depending on how exactly the ferroelectric technology is integrated with the standard process. Since the signal charge per unit area is very large, it is feasible to aggressively scale the lateral dimensions and integrate the ferroelectric capacitor essentially within the contact hole of an MOS transistor as shown in Figure 5a. Using a one transistor/one capacitor cell, as shown schematically in Figure 5b, would allow a nonvolatile static RAM to be built with a density that is better than that of a DRAM.

Figure 5a Advanced FRAM Cell

Integration into CMOS

Figure 5b. Advanced FRAM Cell

IV. Memory Architecture

The basic ferroelectric memory element can be implemented into a memory design in various ways. As mentioned before the early attempts all tried to emulate the magnetic core memory by using a crosspoint array matrix as shown in Figure 2. Although this approach would yield a very dense memory array it failed because of the lack of a well defined and stable coercive voltage. The solution to the above problem is to add a switch to every memory element and thus isolate the nonselected bits from the addressing pulses.
The densest implementation uses one Transistor and one Capacitor per bit (1T/1C), as shown in Figure 5b. The memory architecture chosen to implement this cell is nearly identical to a standard DRAM architecture with the exception that the bottom electrode of the capacitor is pulsed instead of grounded or tied to VCC. A reference such as a dummy cell has to be provided for the differential sensing. A more conservative approach that relaxes the process control requirements is given in Figure 6 which uses a cell with two Transistors and two Capacitors per bit (2T/2C).

![Figure 6. Two Transistor/Two Capacitor Memory Cell](image)

Data is written to the cell by placing true/complement data on the bit lines, selecting a specific cell by activating the word line, and latching the data on the bit lines. This information is then output on the Dout pin (see Figure 8). Since this is a destructive read out, the information is restored to the memory cell by pulsing the plate enable prior to the end of the operation.

![Figure 7. FMX 8101](image)

As a demonstration vehicle, we have designed and fabricated a 256 bit FRAM, the FMX 8101, employing a two transistor, two ferroelectric capacitor memory cell structure as shown in Figure 8. A chip photograph and a block diagram are given in Figures 7 and 8, respectively. As will be shown later, one of the present limitations is the finite number of read cycles permitted. In some applications, the memory would fatigue before it has reached its useful life. To eliminate this problem the FRAM can be operated in a nonvolatile DRAM mode. In this mode the plate enable line (Figure 8) is not activated and the data is stored by charging the ferroelectric capacitor, which acts as a high dielectric constant standard capacitor. This charge must be refreshed periodically (e.g. every four milliseconds) by reading the cell to prevent data loss. Data is read by selecting the word line and transferring the charge to the bit line data latch. At the end of the operation the charge is restored to the cell, refreshing its data. Since this mode the ferroelectric capacitor is not polarized, normal read/write does not impact the ferroelectric cell endurance. However, prior to power down all rows of the memory are read in the nonvolatile FRAM mode to polarize the ferroelectric elements and thus saving the memory contents in a nonvolatile fashion.

Because of the high dielectric constant of PZT, which we measured to be about 1000-1500, it seems feasible to build very high density nonvolatile DRAMs (e.g. 4Mb, 16Mb and beyond) without having to resort to complicated trench processing.

V. Experimental Results

Figures 9 and 10 present some experimental results measured on 256 bit FRAMs and corresponding test capacitors. One of the most intriguing results obtained is probably the extremely fast intrinsic switching speed of the memory device. For all practical purposes the access time of the memory device is given by the basic parameters of the underlying CMOS process. We have attempted to isolate the intrinsic switching time of the PZT layer and believe that it is in the vicinity of 1ns.

A theory of the switching mechanism of PZT has recently been described by Scott et al. [11] who based their work on a model first described by Ishibashi. [12] The model assumes that the switching process is initiated by local nucleation followed by forward and sideways domain growth. It is also assumed that the rate of nucleation is a constant throughout the switching process. Fitting the experimental switching data to this model yields an activation field of order 120KV/cm at room temperature and switching times in the nanosecond range.

![Figure 9. Switched and Non-Switched Charge vs. Time Curves of a 100 x 100µm Ferroelectric Test Capacitor](image)
VI. Conclusions

The ferroelectric technology based on PIIP as the ferroelectric material and combined with a standard semiconductor technology offers the potential to become the “ideal” nonvolatile memory technology. It has been demonstrated that the technology is highly scalable and offers extremely fast intrinsic switching speeds. Nonvolatile semiconductor memories with the speed of static RAMs and the density and cost of DRAMs should be feasible in the near future.

References

[8] Robert W. Vest and Jieje Xu, to be published.