The Asian Test Symposium (ATS) provides an open forum for researchers and industrial practitioners from all countries of the world, especially from Asia, to exchange innovative ideas on system, board, and device testing with design, manufacturing and field consideration in mind.

Scope
Original papers on, but not limited to, the following areas are invited.

- Analog/Mixed-Signal Test
- Automatic Test Generation
- Board Test and Diagnosis
- Boundary Scan Test
- Built-In Self-Test (BIST)
- Defect-Based Test
- Delay and Performance Test
- Dependability and Functional Safety
- Design for Test (DFT)
- Diagnosis and Silicon Debug
- Economic of Test
- Failure Analysis
- Fault Modeling and Simulation
- Fault Tolerance
- GPU Test
- High-Speed I/O Test
- Low-Power IC Test
- Memory Test and Repair
- MEMS Test
- Multi-/Many-core Processor Test
- Nanotechnology Test
- On-line Test
- Power/Thermal/Reliability Issues in Test
- Reconfigurable System Test
- Reliability
- RF Test
- Security and Trust Issues in Test
- Self-Repair
- Sensor Test
- SiP, Stacked, 3D IC Test
- Standards in Test
- Statistical Learning in Test
- Test Compression
- Test Quality
- Test Synthesis
- Validation and Verification
- Yield Analysis and Enhancement

Submissions
Regular Sessions: The ATS’17 Program Committee invites original, unpublished paper submissions on the above topics. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

Key Dates
- Submission deadline: May 26, 2017
- Notification of acceptance: July 31, 2017
- Camera ready manuscript: August 31, 2017