Keynote Address

Embracing Failures

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Abstract
For advanced CMOS technologies, we are now capable of creating billions of transistors per design. Following the economic path of Moore's law, we have integrated new materials at an increasing pace to drive performance, power, and reliability. As layout features went sub-lithography, we have built expertise to fool light. We are integrating vertically with 2.5D/3D packaging. There is research building around monolithic 3D. These advances brought and are continuing to bring significant challenges in dealing with variation. Designers have been managing variation by using adaptive circuit and system approaches for some time. Essentially they have been enabling the design to adapt and accommodate the process capability. This presentation will explore what is a failure in the context of increasing variation and adapting designs and resilient systems. This discussion should challenge assumptions and provoke conversations in testing approaches to economically meet a wide range of market segment requirements.

Speaker’s Bio
John Carulli leads the Test organization at GLOBALFOUNDRIES Fab8 in Malta, NY working on leading edge CMOS technologies. He previously had 21 years at Texas Instruments where he was a Distinguished Member of the Technical Staff. While in the Analog Engineering Operations organization he led test and design data mining methods targeted at test cost reduction. Prior to that in the Silicon Technology Development organization, he was the Manager of the Product Reliability group responsible for product and design reliability activities for new technology development.

John holds 7 US Patents. He has over 50 publications in the areas of reliability, test, and process development. He is co-recipient of two Best Paper Awards and two Best Paper Nominations working in close collaboration with university partners. John serves on the organizing or program committees of several conferences including the International Test Conference, VLSI Test Symposium, and European Test Symposium. He was a recipient of the SRC 2010 Mahboob Khan Outstanding Industry Liaison Award for student mentoring and research collaboration. He is a Senior Member of IEEE. He received his B.S.E.E. and M.S.E.E. degrees from the University of Vermont in Burlington, VT. His research interests include product reliability, outlier analysis, machine learning, performance modeling, logic diagnosis, and security.