Tutorial I

Title: Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems

Presenter: Prof. Krishnendu Chakrabarty
Dept. of Electrical and Computer Engineering,
Duke University

Abstract:
The gap between working silicon and a working board/system is becoming more significant and problematic as technology scales and complexity grows. The result of this increasing gap is failures at the board and system level that cannot be duplicated at the component level. These failures are most often referred to as “NTFs” (No Trouble Founds). The result of these NTFs can range from higher manufacturing costs and inventories to failure to get the product out of the door. The problem will only get worse as technology scales and will be compounded as new packaging techniques (SiP, SoC, 3D) extend and expand Moore’s law. This is a problem that must be solved, yet, little effort has been applied up to this point. This tutorial will provide a detailed background on the nature of this problem and will provide DFT, test, and root-cause identification solutions at the board/system level.

Biography:

Krishnendu Chakrabarty is the William H. Younger Distinguished Professor of Engineering in the Department of Professor of Electrical and Computer Engineering and Professor of Computer Science at Duke University. In addition, he serves as the Executive Director of Graduate Studies in Electrical and Computer Engineering. He is also a Chair Professor at Tsinghua University, Beijing, China. Prof. Chakrabarty is a recipient of the National Science Foundation Early Faculty (CAREER) award, the Office of Naval Research Young Investigator award, the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, and 10 best paper awards at major IEEE conferences. He is also a recipient of the Distinguished Alumnus Award from the Indian Institute of Technology, Kharagpur (2014).

Prof. Chakrabarty’s current research projects include: testing and design-for-testability of integrated circuits; digital microfluidics, biochips, and cyberphysical systems; optimization of digital print and enterprise systems. Prof. Chakrabarty is a Fellow of ACM, a Fellow of IEEE, and a Golden Core Member of the IEEE Computer Society. He holds four US patents and he has several pending patents. He was a 2009 Invitational Fellow of the Japan Society for the Promotion of Science (JSPS). He served as a Distinguished Visitor of the IEEE Computer Society during 2005-2007 and 2010-2012, and as a Distinguished Lecturer of the IEEE Circuits and Systems Society during 2006-2007 and 2012-2013. Currently he serves as an ACM Distinguished Speaker. Prof. Chakrabarty served as the Editor-in-Chief of IEEE Design & Test of Computers during 2010-2012. Currently he serves as the Editor-in-Chief of ACM Journal on Emerging Technologies in Computing Systems. He is also an Associate Editor of IEEE Transactions on Computers, IEEE Transactions on Biomedical Circuits and Systems, and ACM Transactions on Design Automation of Electronic Systems.
Title: Statistical Adaptive Test Methods Targeting 'Zero Defect'
IC Quality and Reliability

Presenter: Prof. Adit D. Singh
Dept. of Electrical and Computer Engineering, Auburn University

Abstract:
Integrated circuits fabricated in aggressively scaled nanometer scale technologies are susceptible to a wide range of random manufacturing defects, some of which can be extremely difficult to reliably detect in post manufacturing testing. Meanwhile commercial applications continue to demand ever higher IC quality, most notably a “zero defect” target from automotive manufacturers. To cost effectively meet these new quality and reliability challenges, innovative new statistical screening techniques and adaptive test methodologies are being developed. These attempt to improve test effectiveness and optimize test costs by identifying “suspect” parts for more extensive testing, using tests specially targeted at the suspected failure mode. Adaptive test methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production digital and analog circuits. Commercial tools offered by a number of new companies that have emerged in the "Adaptive Test" space will also be discussed. Broadly, these aim provide to support for the sharing and leveraging of results from the different tests in the test flow for effective test adaptation and optimization.

Biography:
Adit D. Singh is James B. Davis Professor of Electrical and Computer Engineering at Auburn University, where he directs the VLSI Design and Test Laboratory. His technical interests span all aspects of VLSI test and reliability. He has published nearly two hundred research papers, served as a consultant for several major semiconductor companies, and holds international patents that have been licensed to industry. He has held leadership roles at international test conferences, including serving as General Chair of the 2000 IEEE VLSI Test Symposium, the 2003 IEEE Defect Based Test Workshop, and the 2004 IEEE Memory Test Workshop. He also serves on the editorial boards of IEEE Design and Test Magazine, and JETTA. Dr. Singh is a Fellow of IEEE, a Golden Core member of the IEEE Computer Society and is past chair of the IEEE Test Technology Technical Council. He can be reached at email: adsingh@auburn.edu