Testing Nanoelectronic Circuits Under Massive Statistical Process Variations

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Summary:

The increasing parameter variations in nanoelectronic circuits and systems have led to a paradigm shift towards statistical design. Moreover, variation-tolerant adaptive and self-calibrating systems are steadily gaining importance. Manufacturing test methods have, to this date, failed to adequately incorporate these developments. To keep pace with design trends, efficient test methods are needed coping with the specific challenges due to statistical and variation-tolerant design.

The Special Session will discuss how statistical information can be integrated into known test approaches, such as fault simulation and test pattern generation, and propose dedicated approaches for adaptive and self-calibrating systems. The starting point is an accurate statistical characterization of standard library elements relying both on defect-oriented fault modeling and on a Monte Carlo analysis of the effects of varying process parameters. Exemplary data for 45 nm technology are presented, which have been derived by massive parallel electrical simulation on a large compute cluster and based on industrial input and openly available data. Integrating this information into fault simulation and test pattern generation allows to determine for which parameter configurations a fault can be detected as well as to optimize test patterns, such that faults are detected for a maximum set of parameter configurations. To account for current trends in computer design, the methods are optimized for implementation on state-of-the-art parallel processors such as GPGPUs. The presented tool flows leverage recent improvements in basic algorithms, including last-generation SAT solvers. Adaptive and self-calibrating systems are designed to compensate parameter variations and certain types of failures. Thus, test procedures must be able to distinguish between critical and non-critical failures and avoid miss-classification and yield loss due to overtesting. Furthermore, the actual robustness of the system, i.e. its ability to tolerate faults in the field, must be determined and quantified during manufacturing test. Traditional “pass/fail tests” must be replaced by “quality binning”.