17th Asian Test Symposium

ATS 2008

Table of Contents

Foreword ................................................................................................................................................................. xii
ATS Steering Committee ........................................................................................................................................... xiii
Organizing Committee ................................................................................................................................................ xiv
Program Committee .................................................................................................................................................. xv
Reviewers ............................................................................................................................................................... xvii
TTTC Activities Board ........................................................................................................................................... xviii
Tutorial 1 ................................................................................................................................................................. xxi
Tutorial 2 ............................................................................................................................................................... xxii
ATS 2007 Best Paper Award ................................................................................................................................ xxiii

Session 1: Plenary Session 1

Session 2: Plenary Session 2

Session 3A: Test Data & Response Compression

Not All Xs are Bad for Scan Compression .................................................................................................................. 7
   Anshuman Chandra and Rohit Kapur
Evaluation of Entropy Driven Compression Bounds on Industrial Designs ............................................................. 13
   Srinivasulu Alampally, Jais Abraham, Rubin A. Parekhji, Rohit Kapur, and T.W. Williams

Session 3B: Test Generation and Fault Simulation

Untestable Fault Identification in Sequential Circuits Using Model-Checking ........................................................... 21
   Jaan Raik, Hideo Fujiwara, Raimund Ubar, and Anna Krivenko
A Test Generation Method for State-Observable FSMs to Increase Defect Coverage under the Test Length Constraint ................................................................................................................................. 27
   Ryoichi Inoue, Toshinori Hosokawa, and Hideo Fujiwara
LIFTING: A Flexible Open-Source Fault Simulator .................................................................................................... 35
   Alberto Bosio and Giorgio Di Natale


Session 3C: RF Testing
Digitally-Assisted Analog/RF Testing for Mixed-Signal SoCs ................................................................. 43
    Hsiu-Ming (Sherman) Chang, Min-Sheng (Mitchell) Lin, and Kwang-Ting (Tim) Cheng
Low-Cost One-Port Approach for Testing Integrated RF Substrates .......................................................... 49
    Abhilash Goyal and Madhavan Swaminathan
Efficient Low-Cost Testing of Wireless OFDM Polar Transceiver Systems ................................................... 55
    Deuk Lee, Vishwanath Natarajan, Raj Senguttuvan, and Abhijit Chatterjee

Session 4A: Test Compression and BIST
Interconnect-Driven Layout-Aware Multiple Scan Tree Synthesis for Test Time, Data Compression and Routing Optimization .......................................................................................................................... 63
    Katherine Shu-Min Li and Jr-Yang Huang
Sequential Circuit BIST Synthesis Using Spectrum and Noise from ATPG Patterns ................................................................. 69
    Nitin Yogi and Vishwani D. Agrawal
A Novel BIST Scheme Using Test Vectors Applied by Circuit-under-Test Itself .......................................................................................................................... 75
    Jishun Kuang, Xiong Ouyang, and Zhiqiang You

Session 4B: Test Generation for Physical Faults
XPDF-ATPG: An Efficient Test Pattern Generation for Crosstalk-Induced Faults ................................................................. 83
    Sunghoon Chun, Yongjoon Kim, Taejin Kim, Myung-Hoon Yang, and Sungho Kang
A Multi-valued Algebra for Capacitance Induced Crosstalk Delay Faults ................................................................. 89
    Arani Sinha, Sandeep K. Gupta, and Melvin A. Breuer
Increasing Defect Coverage by Generating Test Vectors for Stuck-Open Faults ................................................... 97
    Yoshinobu Higami, Kewal K. Saluja, Hiroshi Takahashi, Shin-ya Kobayashi, and Yuzo Takamatsu

Session 4C: Analog and Mixed-Signal Test
Technique to Improve the Performance of Time-Interleaved A-D Converters with Mismatches of Non-linearity ................................................................. 105
    Koji Asami, Hidetaka Suzuki, Hiroyuki Miyajima, Tetsuya Taura, and Haruo Kobayashi
A Reduced Code Linearity Test Method for Pipelined A/D Converters ................................................................. 111
    Jin-Fu Lin, Te-Chieh Kung, and Soon-Jyh Chang
Testing LCD Source Driver IC with Built-on-Scribe-Line Test Circuitry ................................................................. 117
    Jui-Jer Huang, Chiuan-Che Li, and Jian-Lang Huang
Session 5A: Delay Testing

Identifying Non-Robust Untestable RTL Paths in Circuits with Multi-cycle Paths ................................................................. 125
   Thomas Edison Yu, Tomokazu Yoneda, Satoshi Ohtake, and Hideo Fujiwara
High Quality Pattern Generation for Delay Defects with Functional Sensitized Paths ......................................................... 131
   Ming-Ting Hsieh, Shun-Yen Lu, Jing-Jia Liou, and Augusli KiFli
Refining Delay Test Methodology Using Knowledge of Asymmetric Transition Delay ............................................................ 137
   Sean H. Wu, Sreejit Chakravarty, Alexander Tetelbaum, and Li-C. Wang

Session 5B: Special Session: Analog Production Test 1

Effects of Advances in Analog, Mixed Signal and IO Circuits on Test Strategies ............................................................... 145
   Salem Abdennadher
Electrical Overstress Prevention & Test Best Practices ......................................................... 146
   Leslie Khoo
Low Distortion Sine Waveform Generation by an AWG .......................................................... 147
   Akinori Maeda

Session 5C: Hybrid Method for Test Data Compression

An Effective Hybrid Test Data Compression Method Using Scan Chain Compaction and Dictionary-Based Scheme ..................... 151
   Taekin Kim, Sunghoon Chun, Yongjoo Kim, Myung-Hoon Yang, and Sungho Kang
Optimizing Test Data Volume Using Hybrid Compression .................................................................................................... 157
   Brion Keller, Sandeep Bhatia, Thomas Bartenstein, Brian Foutz, and Anis Uzzaman
Cost Efficient Methods to Improve Performance of Broadcast Scan .......................................................................................... 163
   Seongmoon Wang and Wenlong Wei

Session 6A: Fault Diagnosis

Hyperactive Faults Dictionary to Increase Diagnosis Throughput ......................................................................................... 173
   Chen Liu, Wu-Tung Cheng, Huaxing Tang, Sudhakar M. Reddy, Wei Zou, and Manish Sharma
Enhancing Transition Fault Model for Delay Defect Diagnosis ............................................................................................... 179
   Wu-Tung Cheng, Brady Benware, Rui Feng Guo, Kun-Han Tsai, Takeo Kobayashi, Kazuyuki Maruo, Michinobu Nakao, Yoshiaki Fukui, and Hideyuki Otake
Observation Point Oriented Deterministic Diagnosis Pattern Generation (DDPG) for Chain Diagnosis ................................... 185
   Fei Wang, Yu Hu, Yu Huang, Jing Ye, and Xiaowei Li
Session 6B: Special Session: Analog Production Test 2

The HiZ Problem of Power Management IC Testing ............................................................... 193
   Hagen Goller

Total Jitter Measurement for Testing HSIO Integrated SoCs ........................................ 194
   Takahiro J. Yamaguchi and Masahiro Ishida

Load-Board/PCB Noise Suppression via Electromagnetic Band Gap Power Plane Patterning ............................................................................................................................... 195
   Fidel Muradali, Suzanne Huh, and Madhavan Swaminathan

Session 6C: Defect Based Testing

Defect Detection Rate through IDDQ for Production Testing ........................................... 199
   Junichi Hirase

Variation Aware Analysis of Bridging Fault Testing ........................................................................ 206
   Urban Ingelsson, Bashir M. Al-Hashimi, and Peter Harrod

Prioritizing the Application of DFM Guidelines Based on the Detectability of Systematic Defects .......................................................................................................................... 212
   Dongok Kim, Irith Pomeranz, M. Enamul Amyeen, and Srikantan Venkataraman

Session 7A: Panel: How to Increase the Effectiveness of Yield Diagnostics - Is DFM the Answer to This?

How To Increase the Effectiveness of Yield Diagnostics - Is DFM the Answer to This? ................................................................. 221
   Anis Uzzaman

Session 7B: Power Aware Test Generation

Targeting Leakage Constraints during ATPG ........................................................................ 225
   Görschwin Fey, Satoshi Komatsu, Yasuo Furukawa, and Masahiro Fujita

Power Management for Wafer-Level Test During Burn-In ............................................. 231
   Sudarshan Bahukudumbi and Krishnendu Chakrabarty

Test Generation for State Retention Logic ........................................................................ 237
   Krishna Chakravadhanula, Vivek Chickermane, Brion Keller, Patrick Gallagher, and Steven Gregor

Session 7C: Design for Efficient Test

Area and Test Cost Reduction for On-Chip Wireless Test Channels with System-Level Design Techniques ................................................................................................................................. 245
   Chun-Kai Hsu, Li-Ming Deng, Mao-Yin Wang, Jing-Jia Liou, Chih-Tsun Huang, and Cheng-Wen Wu

On-Chip Test Generation Mechanism for Scan-Based Two-Pattern Tests ...................... 251
   Nan-Cheng Lai and Sying-Jyan Wang

Level-Testability of Multi-operand Adders ......................................................................... 257
   Nobutaka Kito and Naofumi Takagi
Session 8A: Industry Session

System Level LBIST Implementation ................................................................. 263
  Fei Zhuang, JunBo Jia, and Xiangfeng Li
CooLBIST: An Effective Approach of Test Power Reduction for LBIST ................ 264
  Jun Matsushima, Yoichi Maeda, and Masahiro Takakura
Practical Challenges in Logic BIST Implementation – Case Studies .................. 265
  Shianling Wu, Hiroshi Furukawa, Boryau Sheu, Laung-Terng Wang, Hao-Jan Chao,
  Lizhen Yu, Xiaqiong Wen, and Michio Murakami
USB2.0 Logic Built In Self Test Methodology .................................................. 266
  Kean Hong Boey, Kok Sing Yap, and Wai Mun Ng
Shared At-Speed BIST for Parallel Test of SRAMs with Different Address Sizes .................................................................................................................... 267
  Tomonori Sasaki, Yoshiyuki Nakamura, and Toshiharu Asaka
Experimental Results of Built-In Jitter Measurement for Gigahertz Clock .......... 268
  Nai-Chen Daniel Cheng, Yu Lee, and Ji-Jan Chen
Leading Edge Technology and Test Noise ....................................................... 269
  Katayama Takayuki, Kou Ebihara, and Goro Imaizumi
DFT Technique to Conclusively Translate Floating Nodes to High IDDQ ......... 270
  Ricky Smith and Jiang Shi
Diagnosis of Voltage Dependent Scan Chain Failure Using VBUMP Scan Debug Method .................................................................................................................... 271
  Khairul Khusyari, Wei Tee Ng, Neal Jaarsma, Robert Abraham, Peng Weng Ng,
  Boon Hui Ang, and Chin Hu Ong
Detectability of the Two-Dimensional Detector for Time Resolved Emission Measurement ..................................................................................................................... 272
  Nobuyuki Hirai
Protocol Aware Test Methodologies Using Today’s ATE ................................ 273
  Shawn Molavi, Andy Evans, and Ray Clancy

Session 8B: SoC Test

Core-Level Compression Technique Selection and SOC Test Architecture Design ................................................................. 277
  Anders Larsson, Xin Zhang, Erik Larsson, and Krishnendu Chakrabarty
Simulation-Driven Thermal-Safe Test Time Minimization for System-on-Chip .................................................. 283
  Zhiyuan He, Zebo Peng, and Petru Eles
A Design-for-Debug (DfD) for NoC-Based SoC Debugging via NoC .................. 289
  Hyunbean Yi, Sungiu Park, and Sandip Kundu
Accelerated Functional Testing of Digital Microfluidic Biochips ....................... 295
  Debasis Mitra, Sarmishtha Ghoshal, Hafizur Rahaman, Bhargab B. Bhattacharya,
  D. Dutta Majumder, and Krishnendu Chakrabarty
Session 8C: Design Verification and Validation

On Reusing Test Access Mechanisms for Debug Data Transfer in SoC
Post-Silicon Validation .................................................................303
  Xiao Liu and Qiang Xu
A Robust Automated Scan Pattern Mismatch Debugger ........................................309
  Kun-Han Tsai, Ruifeng Guo, and Wu-Tung Cheng
An Interactive Verification and Debugging Environment
by Concrete/Symbolic Simulations for System-Level Designs ................................315
  Yoshihisa Kojima, Tasuku Nishihara, Takeshi Matsumoto, and Masahiro Fujita
Coverage Directed Test Generation: Godson Experience ........................................321
  Haihua Shen, Wenli Wei, Yunji Chen, Bowen Chen, and Qi Guo

Session 9A: Power Aware Scan Test

Test Power Reduction by Blocking Scan Cell Outputs ..................................................329
  Xijiang Lin and Janusz Rajski
Two-Gear Low-Power Scan Test .................................................................................337
  Chao-Wen Tzeng and Shi-Yu Huang
DCScan: A Power-Aware Scan Testing Architecture ..................................................343
  Gui Dai, Zhiqiang You, Jishun Kuang, and Jiedi Huang

Session 9B: Memory Self Test

Layout-Aware and Programmable Memory BIST Synthesis for Nanoscale
System-on-Chip Designs .........................................................................................351
  Aman Kokrady, C.P. Ravikumar, and Nitin Chandrachoodan
A Low-Cost Pipelined BIST Scheme for Homogeneous RAMs in Multicore
Chips ..............................................................................................................357
  Yu-Jen Huang and Jin-Fu Li
A Software-Based Test Methodology for Direct-Mapped Data Cache ................................363
  Yi-Cheng Lin, Yi-Ying Tsai, Kuen-Jong Lee, Cheng-Wei Yen, and Chung-Ho Chen

Session 9C: On-Line Test

Time-Multiplexed Online Checking: A Feasibility Study ........................................371
  Ming Gao, Hsiu-Ming (Sherman) Chang, Peter Lisherness, and Kwang-Ting (Tim) Cheng
On-Line Instruction-Checking in Pipelined Microprocessors ........................................377
  Stefano Di Carlo, Giorgio Di Natale, and Riccardo Mariani
Design of FSM with Concurrent Error Detection Based on Viterbi Decoding .................383
  Li Ming, Xu Shiyi, Xia Enjun, and Wan Fayu
Session 10A: Power Aware Delay Testing

PHS-Fill: A Low Power Supply Noise Test Pattern Generation Technique for At-Speed Scan Testing in Huffman Coding Test Compression

Yi-Tsung Lin, Meng-Fan Wu, and Jiun-Lang Huang

CTX: A Clock-Gating-Based Test Relaxation and X-Filling Scheme for Reducing Yield Loss Risk in At-Speed Scan Testing


Power Analysis and Reduction Techniques for Transition Fault Testing

Khushboo Agarwal, Srinivas Vooka, Srivaths Ravi, Rubin Parekhji, and Arjun Singh Gill

Session 10B: Advanced Memory Test

Influence of Parasitic Capacitance Variations on 65 nm and 32 nm Predictive Technology Model SRAM Core-Cells

Stefano Di Carlo, Alessandro Savino, Alberto Scionti, and Paolo Prinetto

Test and Diagnosis Algorithm Generation and Evaluation for MRAM Write Disturbance Fault

Wan-Yu Lo, Ching-Yi Chen, Chin-Lung Su, and Cheng-Wen Wu

GDDR5 Training – Challenges and Solutions for ATE-Based Test

Hubert Werkmann, Dong-Myong Kim, and Shinji Fujita

Session 10C: Fault Tolerance and Dependable System

A Re-design Technique for Datapath Modules in Error Tolerant Applications

Doochul Shin and Sandeep K. Gupta

Reliable Network-on-Chip Router for Crosstalk and Soft Error Tolerance

Ying Zhang, Huaweí Li, and Xiaowei Li

Analyses on Trend of Accidents in Financial Information Systems Reported by Newspapers from the Viewpoint of Dependability

Koichi Bando and Kenji Tanaka

Author Index

Call for Papers ATS 2009