The Application of BIST-Aided Scan Test for Real Chips

Hideaki Konishi, Michiaki Emori, Takahisa Hiraide
FUJITSU LIMITED
1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki, 211-8588, Japan
{hideaki.konishi, emori.michiaki, hiraide.takahisa}@jp.fujitsu.com

Abstract
It is common to use ATPG of scan–based design for high fault coverage in LSI testing. However, significant increase in test cost is caused in accordance with increasing design complexity. We proposed a new method, BIST-Aided Scan Test (BAST), to reduce test cost in 2003[1]. Since then, we applied this method for about 200 chips, and the result is very successful to reduce test cost with less design flow impact.

1. Concept
In many cases, deterministic test patterns generated by ATPG consist of a large number of don’t-care bits and a small number of care bits. In case of BAST, the random values that are assigned by ATPG are internally generated by PRPG. The remaining specified values are encoded to apply through the interface channels between the ATE and the CUT. Therefore, a large part of test data can be omitted on the ATE storage. In addition, the MISR eliminates the need for the whole expected signals in the ATE. The usage of a MISR requires of BAST to handle the problem of X-states(unknown states) that corrupt the signature. Therefore, BAST has a function for masking the ill effect of X-states.

2. Design Flow
The followings are the general design flow and extra work for BAST.
- DFT ... BAST logic insertion
- DRC ... BAST structure check
- layout/STA ... BAST circuit timing check
- ATPG ... Test pattern generation with PRPG
- Validation ... Parallel load simulation for BAST
This shows BAST affect low impact in test flow and requires no need for test point insertion and mask logic insertion for X-states.

3. Results
We applied BAST to many real chip designs. The followings are examples of them. The results for test time and test data are shown in table 1 and table 2. The circuit 1 is 7.9Mgates with 270k flip flops. The circuit 2 is the 4.0Mgates with 150k flip flops. The circuit 3 is 18Mgates with 425k flip flops. The BAST hardware overhead is 0.2%, 0.3% and 0.1% for each circuit, compared with the conventional scan-based design.
The results show test data is reduced to 1/22, 1/18 and 1/22, and the test time is reduced to 1/12, 1/9 and 1/17 for each circuit. The fault coverage is 99.69%, 99.78% and 100.00% for each circuit, and they are enough high and the same with the conventional method with ATPG for scan-based design.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Original test data size</th>
<th>BAST test data size</th>
<th>Reduction ratio of test data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit1</td>
<td>2068MB</td>
<td>93MB</td>
<td>1/22</td>
</tr>
<tr>
<td>Circuit2</td>
<td>2439MB</td>
<td>139MB</td>
<td>1/18</td>
</tr>
<tr>
<td>Circuit3</td>
<td>455MB</td>
<td>21MB</td>
<td>1/22</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Original test time</th>
<th>BAST test time</th>
<th>Reduction ratio of test time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit1</td>
<td>112.2Mcycle</td>
<td>9.0Mcycle</td>
<td>1/12</td>
</tr>
<tr>
<td>Circuit2</td>
<td>132.9Mcycle</td>
<td>14.5Mcycle</td>
<td>1/9</td>
</tr>
<tr>
<td>Circuit3</td>
<td>22.3Mcycle</td>
<td>1.3Mcycle</td>
<td>1/17</td>
</tr>
</tbody>
</table>

4. Summary
We proposed BAST to reduce test cost reduction method in 2003. BAST enables drastic test cost reduction with keeping high fault coverage. BAST also affect low impact in test design flow and requires no need for test point insertion and mask logic insertion for X-states. Therefore, BAST has been accepted by many designers, and applied for about 200 designs.

5. References