Mentor Graphics DFT to Navigate Nanometer Test Challenges

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Abstract

Nanometer designs are getting smaller and bigger. Feature sizes are moving into nanometer geometries. Semiconductor companies creating these nanometer designs are struggling with many issues that result from this shrinking complex design environment. Mentor Graphics Design-For-Test is committed to helping you navigate these challenges to bringing a high quality product to market while reducing test cost.

1 Introduction

When it comes to test, the semiconductor industry is hitting the wall. Scan and the "stuck-at" fault model have been the standard for semiconductor test for more than a decade, but as system-on-chip (SOC) designs move to 90 nm and below, manufacturing test will undergo significant changes. Standard "stuck-at" tests alone will no longer be sufficient to ensure test quality and target defect rates. To remain competitive and ensure that quality parts are delivered to end customers, semiconductor companies across the board will need to reconsider their test strategies and upgrade their methodologies.

2 Test Challenges

- Test Quality

The first and main purpose of testing is to provide a high quality test which reduces the escapes or defective products from being shipped as good. Our development in this area involved tests that would supplement a stuck-at, memory BIST, and macro test strategy. At-speed scan testing has become a necessity at many companies with high quality requirements or if they are producing 90 nm or smaller technology designs. Multiple detect tests have been proven to improve the detection of bridging faults and improve DPM rates. Defect-based test will take physical properties into consideration to produce tests that specifically target potential defects. In addition, we are continually investigating other new fault models that may help improve test quality.

- Test Cost

Increasing test quality is vitally important but it must be done while reducing the impact to the total cost of test which includes silicon area, design cycle time, tester memory and tester time. The industry has already seen excellent success with the embedded deterministic test (EDT) compression within TestKompress. Further improvements are in process. The core ATPG dynamic compaction is also being improved so that more faults can be detected with each pattern, thus reducing the total pattern count for both TestKompress and FastScan.

- Productivity

 Our third focus area is to improve how our tools fit into our customers’ design flows and make the designers’ tasks easier. There are recent and upcoming improvements to tool performance (run time). Features to support modular or block-based flows are soon to be available. Finally, our debug environment is undergoing a major update to ease the task of troubleshooting design rules failures and low coverage.

- Time-to-Market

Processing and interpreting test failure data has a significant impact on the Time-to-Market of a product. Additionally, the time to perform failure analysis (FA) is critical to bringing a product to high volume production and profitability. Our tools provide diagnostics to report defect candidates based on failing test patterns. These features are being expanded to isolate new fault models and simplify the use of diagnostics. Our linkage with the Calibre tool also allows our customers to link diagnostic data to the physical design and provide more timely resolution of yield problems.

3 Conclusions

Mentor has been focused on in DFT for almost 15 years now with products like FastScan, TestKompress, LBISTArchitect and MBISTArchitect.

The next frontier for us is to link our diagnostics capabilities with physical information and the Calibre platform and expand further into yield learning and yield enhancement. Because Mentor has a leadership position in both test and physical verification, we are in an ideal position to capitalize on this market. FastScan, TestKompress and Calibre are all market leading products and building on their strength gives us a distinct advantage.