Test-Point Selection Algorithm Using Small Signal Model for Scan-Based BIST

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Abstract

A test point selection algorithm TEPSAUS (TEst-Point Selection Algorithm Using Small signal model) for scan based build-in self-test (BIST) is proposed in this paper. In order to reduce the computational complexity, the algorithm uses Small Signal Model (SSM) to build recursion formulas for cost reduction functions. With the recursion functions, the cost reduction functions can be calculated efficiently.

1. Small signal model

In [1], a metric is defined as

\[ U = \frac{1}{|M|} \sum_{j \in M} \frac{1}{Pd_j} \]  \hspace{1cm} (1)

where \( M \) is the fault set, \(|M|\) is the cardinality of \( M \). \( Pd_j \) is the detection probability of fault \( j \) under the stuck-at fault model, the probability of detecting a fault on line \( i \) is

\[ Pd_{i,0} = P_{i,0} \cdot O_i \] \hspace{1cm} \text{Stuck-At-Zero Fault} \hspace{1cm} (2)

\[ Pd_{i,1} = (1-P_{i,0}) \cdot O_i \] \hspace{1cm} \text{Stuck-At-One Fault} \hspace{1cm} (3)

When a test point is added to the CUT, it will disturb some signals' controllability and observability. Such disturbances will cause the disturbance on \( U \) [1]. The relationship between the disturbance on \( U \) and the disturbances on controllability and/or observability is non-linear. If the disturbances on controllability and/or observability are small enough, the disturbance on \( U \) could be expressed as a linear formula, which can be used to build the recursion function. The calculation time is then shortening down with this small signal model. In the following section, a test-point selection algorithm is proposed based on the small signal model.

2. Recursion formulas for cost reduction function

In Figure 1, assuming \( O_{k+1,i} = O_{k,i} + \Delta O_{k+1,i} \) and \( C_{k,i,j} = \min(C_{k,i,j,1}, C_{k,i,j,0}) \), where \( O_{k,i} \) is the observability of node \( N_{k,i} \), \( C_{k,i,j,1} \) and \( C_{k,i,j,0} \) are the controllabilities of ‘1’ and ‘0’ for \( N_{k,i} \), respectively, then

\[ \Delta U_{k+1,i} = \frac{1}{C_{k,i,j,0} \cdot O_{k+1,i}} + \sum_{j} (A_{k,i,j} \cdot B_{k,i,j} \cdot \Delta U_{k,j}) \] \hspace{1cm} (4)

\[ A_{k,i,j} = \prod_{m \neq j} (1-(\prod_{m \neq j} C_{k,m,j,x} \cdot O_{k+1,m})) \]

\[ B_{k,i,j} = (\prod_{m \neq j} C_{k,m,j/x}) \]

Where \( C_{k,i,j/x} \) equals to \( C_{k,i,j,1} \) for AND or NAND gates and \( C_{k,i,j,0} \) for OR or NOR gates.

Figure 2 shows the controllability of a node when a little change \( \Delta C_{k,i,j} \) occurs on node \( N_{k,i} \). Assuming

\[ C_{k,i,j} = C_{k,i,j,0} + \Delta C_{k,i,j} \]

\[ \Delta U_{k,i,j} = \frac{1}{O_{k,i,j} \cdot C_{k,i,j}} \]

\[ + \sum_{j \neq i} (A_{k,i,j} \cdot O_{k-1,j} \cdot (\prod_{m \neq j} C_{k,m,j,x}) \cdot \Delta U_{k,j}) \hspace{1cm} (k = 1, 2, ..., n) \]

\[ + (\prod_{j \neq i} C_{k,i,j}) \cdot \Delta U_{k-1,i} \] \hspace{1cm} (5)

3. Conclusion

TEPSAUS has been applied on many benchmarks. The experimental results show that TEPSAUS can find global optimal test points for ISCAS89 benchmarks and b14, b15 of ITC99 benchmark, and the CPU time is significantly reduced.

4. Reference: