Tutorial 2: SoC Testing and P1500 Standard

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Tutorial Summary
Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. This tutorial presents the state-of-the-art in system-level integration and addresses the strategies and current industrial practices in the test of system-on-chip. It discusses the requirements for test reuse in hierarchical design, such as embedded test strategies for individual cores, test access mechanisms, test interface standardization, optimizing test resource partitioning, and embedded test management and integration at the System-on-Chip level.

Tutorial Program
The tutorial program will specifically contain:
1. Introduction
2. Embedded Test Strategies for Cores
3. Test Interface and Access Mechanisms
4. Test Resource Partitioning
5. Embedded Test Integration for SOC
6. SOC Test and Beyond
7. Conclusion

Presenter’s Biography
Yervant Zorian is the Chief Technology Advisor of LogicVision Inc. Previously, he was a Distinguished Member of Technical Staff at Bell Labs, Lucent Technologies, Test and Reliability Center of Excellence. His activities include the areas of embedded core, IC and Multi-Chip Module DFT methodologies. Zorian received an MSc degree from the University of Southern California, and a PhD from McGill University. He is currently the Editor-in-Chief of IEEE Design & Test of Computers. He founded and chairs the TECS workshop; and the IEEE P1500 Embedded Core Test Standardization Working Group. He has provided tutorials and courses at numerous conferences and academic programs (such as ITC, ICCAD, DATE, VTS, ETW, etc). He was granted several patents in the domain of embedded test and received a number of Best Paper Awards. He is a Fellow of IEEE.