Tutorial 1: High Performance/Delay Testing

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Tutorial Summary

Manufacturing defects and process variations cause a manufactured device to fail performance requirements. Defects and process variations causing these failures are detected and diagnosed by testing for delay defects. Several fault models have been proposed to capture the effect of the delay defects. These include transition faults, gate delay faults, and path delay faults. Delay defects may cause some circuit paths to exhibit larger than expected delays as well smaller than expected delays. The latter defects are called short delay defects and the former are called long delay defects.

In this tutorial we will discuss fault models, fault simulation, test generation, design for test methods, and built-in-self test methods. Methods to handle the enormous numbers of paths in large circuits called non-enumerative methods will also be discussed.

Tutorial Program

1. Introduction
2. Fault models
3. Classification of tests
4. Fault simulation
5. Test generation
6. Selection of faults to be tested
7. Design for testability
8. Built-in-self test
9. Non-enumeration techniques

Presenter’s Biography

Sudhakar Reddy obtained his undergraduate degree in Electrical and Communication Engineering from Osmania University, M.S. degree from Indian Institute of Science, and Ph.D. degree in Electrical Engineering from the University of Iowa, Iowa City, Iowa. Dr. Reddy has been active in the areas of testable designs and test generation for logic circuits since 1972. He has been an associate editor and twice a guest editor of IEEE Transactions on Computers. He was Program Committee Chair for 1989 International Symposium on Fault-tolerant Computing. Since 1968 he has been a member of the faculty of the Department of Electrical and Computer Engineering, University of Iowa, where he is currently the Department Chairman. In 1990 he was made a University of Iowa Foundation Distinguished Professor. In 1995 he received the Von Humboldt Senior Researcher Fellowship. He is currently an associate editor of IEEE Transactions on CAD. He is a Fellow of IEEE.

Dr. Reddy has served on the Technical Advisory Board of Sunrise Test Systems. He has been a consultant to Honeywell Inc, AT&T Bell Labs, Rockwell-Collins, and Mentor Graphics. Dr. Reddy has presented tutorials on Delay Fault Testing at International Test Conference for several years.