Testing in the Fourth Dimension

Vishwani D. Agrawal
Bell Labs
Murray Hill, NJ 07974
va@research.bell-labs.com

Abstract

Digital testing in the last three decades has taught us the value of design for testability (DFT). Disciplines such as scan and built-in self test (BIST) have emerged as standard practices because they allow logic testing of arbitrarily large systems. This has been one of the greatest achievements in testing thus far. These past decades have also produced significant advances in semiconductor technology, which make extremely fine features and larger scales of integration possible. The beginning of the new millennium is an era of the system-on-a-chip (SOC). Today’s specialized SOCs will soon become large-volume production chips and there will lie our testing challenge of the new millennium.

Those SOCs will contain mixed signal subsystems. Testing of analog parts has always required accurate generation and analysis of timing waveforms. Digital subsystems of the future SOCs can be characterized as ultra-high speed devices whose clock-rates will exceed any affordable automatic test equipment (ATE). Besides, the signal integrity of ATE to device under test interface will be a major source of yield loss. If we can learn from the experience of the past, DFT, though not necessarily the same DFT, should be the answer I do not mean that a BIST-based speed test will have the ATE go away. I think the future design styles will explore new DFT methods for timing test that are similar to scan only in spirit. For example, high-speed clocks and other time-critical waveforms may be generated on chip by locally embedded circuitry (modified flip flops, DSP, filters, etc.). So, the challenge for the future is to find a timing analog of “scan” that will allow both logic and timing tests of arbitrarily complex systems and also permit simple tests to ascertain the integrity of the DFT hardware.

Vishwani D. Agrawal is a Distinguished Member of Technical Staff at Bell Labs, Murray Hill, New Jersey, USA, and a Visiting Professor at Rutgers University, New Brunswick, New Jersey, USA. He received a BSc degree from Allahabhad University, Allahabad, India, in 1960, BE degree from University of Roorkee, Roorkee, India, in 1964, ME degree from the Indian Institute of Science, Bangalore, India, in 1966, and a PhD degree from the University of Illinois at Urbana-Champaign in 1971. In 1986, he was elected an IEEE Fellow for his contributions to “probabilistic testing of integrated circuits”. In 1993, University of Illinois honored him with their Distinguished Alumnus Award. In 1998, he received the Harry H. Goode Award of the IEEE Computer Society for “innovative contributions to the field of electronic testing”. He has published 250 papers and five books, and has received five best paper awards. He holds twelve U.S. patents on testing and low-power design. He has co-directed 12 PhD theses at major universities. In 1991 he co-founded the International Conference on VLSI Design. He is a former editor-in-chief (1985-87) of the IEEE Design & Test of Computers and the founding editor-in-chief (since 1990) of the Journal of Electronic Testing: Theory and Applications. He was the program chair for the Fourth IEEE Asian Test Symposium. He serves on the ECE Alumni Board of the University of Illinois and the ECE Advisory Board of the New Jersey Institute of Technology.