A Current Testing for CMOS Logic Circuits Applying Random Patterns and Monitoring Dynamic Power Supply Current

Hideo TAMAMOTO, Hiroshi YOKOYAMA and Yuichi NARITA
Department of Information Engineering, Akita University
Akita City, Akita 010 Japan

Abstract
Assuming a stuck-at fault and stuck-open fault, we discussed a random current testing for CMOS logic circuits by monitoring a dynamic power supply current. Random patterns are generated using a modified LFSR, where the outputs of a CUT are fed back to an LFSR. This modification is intended for amplifying the influence of a fault near a primary outputs on the dynamic current.

Simulation results showed that the modified LFSR works well for detectability, and a high fault coverage can be obtained applying a small number of test vectors.

1. Introduction
In a traditional testing for a logic circuit, the internal state of the circuit is examined by applying test vectors to primary inputs and then observing their responses at primary outputs. However, with the increase of integration of a circuit, it becomes difficult to examine the internal state by checking the relationship between test vectors and their responses, because external lines do not so increase although the internal structure has become very complex. Some methods were proposed to meet with this difficulty, which make the circuit highly observable by using an EB prober[1], or by monitoring a power supply current. The testing based on the latter method is called current testing[2-9]. It is known that when a fault occurs in a CMOS logic circuit, the power supply current in a quiescent state (static current), which is usually very small, may increase. The current testing method monitoring this static current is called IDDQ testing, and has been received much attention as a promising method[2,3]. This is because the faults missed by a traditional stuck-at fault testing can be detected, test vectors can be easily generated and so on. Since the static current has to be monitored after the operating state of a circuit under test (CUT) becomes steady, the testing rate is usually slow[8].

Whenever test vectors are applied to a CUT, the transitions of logical values occur at the output of some gates. The appearances of transitions in a faulty circuit, in general, differ from the ones of a fault-free circuit. In a CMOS logic circuit, a dynamic power supply current (dynamic current) flows at a gate, when a transition occurs. Hence, by monitoring the dynamic current of a CUT, we can know whether a fault occurs or not.

In a current testing, it is not always necessary to propagate a fault information to a primary output, but it is only sufficient to sensitize a fault. This is because a current testing is one such that the internal state of a CUT can be indirectly observed by means of a power supply current. So we consider that a current testing can be effectively performed even if random patterns are applied to a CUT.

In this paper, assuming a stuck-at fault and a stuck-open fault, we discuss a current testing for a CMOS combinational logic circuit where random patterns are applied as test vectors and the dynamic current is monitored. The dynamic current can be monitored without waiting for the operating state of a CUT to become steady. Therefore, this current testing can be performed faster than the one by monitoring the static current.

In order to detect a fault by means of an obvious change of the dynamic current, the fault information has to be widely spread in a CUT. This is because the appearances of transitions have to be sufficiently affected by a fault. The information of a fault near a primary input may be widely spread in a CUT, but the one near a primary output may not. We have to devise some method to cause the information of a fault near a primary output to be widely spread. We discussed the method that random patterns are generated using a modified LFSR, where the outputs of a CUT are fed back to an LFSR[10]. Since the information of a fault near a primary output may be easily propagated to a primary output, the information of the fault may be widely spread through the modified LFSR.

In order to detect a fault, it is necessary that the dynamic current of a faulty circuit has to be distinguished from the one of a fault-free circuit. We consider that the mean value represents some feature of the the dynamic current, and discuss the distinguishing scheme that the mean dynamic current of a CUT is compared with the one measured in a fault-free circuit.

Simulation results showed that a high fault coverage can be obtained by applying a small number of test vectors.
vectors, and the proposed current testing proved to be a promising candidate of a testing method for a CMOS logic circuit.

2. Fault Model

We consider a combinational logic circuit composed of CMOS gates. We assume a single stuck-at fault, and a single stuck-open fault of a transistor constituting a gate.

When a logical value at the output of a gate is changed from one to zero or from zero to one, the inputs of the succeeding gates are charged or discharged, respectively, and at this time the dynamic current flows. If a fault occurs, when a test vector is applied, the locations where a transition occurs and/or the number of transitions occurring in a CUT are, in general, different from the ones of a fault-free circuit. Therefore, the dynamic current of a faulty circuit may be different from the one of a fault-free circuit. This is the basic idea which underlies our current testing.

The propagation delay of signals usually exists in a logic circuit. If this delay is considered, it seems that the transition which occurs at the output of any gate is propagated along the path leading from there to a primary output one after another. If some transitions reconverge at any gate after they are propagated along several paths with different length, a hazard may occur\[11]. The appearances of transitions become more complex than the ones in case the delay does not exist. It is interesting to investigate whether the delay works well for detectability or not.

In a high-speed IC, the delay occurring on a signal line cannot be neglected. However, since this delay is strongly dependent on the layout of the wiring, it is difficult to estimate its influence precisely. So we consider the gate delay only in this paper.

3. Testing circuit and testing method

The circuit configuration of our proposed current testing scheme is shown in Fig. 1. The circuit consists of a random pattern generator (FPG) for applying test vectors, and a processor for fault detection by analyzing the monitored dynamic current.

3.1 Pseudo-random pattern generator

Test vectors are generated using a modified LFSR, named a feedback pattern generator (FPG), where the outputs of a CUT are fed back to the registers (latches) of an LFSR through EOR gates. Fig. 2 shows an example of the FPG that can be used for a CUT having five primary inputs and two primary outputs. This FPG may generate some sequence of pseudo-random patterns. If the length of the sequence is not so long that the random patterns cannot be used as test vectors, the length of the sequence must be made longer by increasing the stages of an LFSR.

![Fig. 2 An example of the FPG for a circuit having five primary inputs and two primary outputs.](image)

3.2 Fault detection

In order to detect a fault by means of an obvious difference of the dynamic current, the fault information has to be widely spread in a CUT. This is because the appearances of the transitions are sufficiently affected and the dynamic current may be different from the one of a fault-free circuit. If a fault occurs near a primary input, the fault information may be widely spread in a circuit, even though the fault information may not be propagated to a primary output. If a fault occurs near a primary output, the fault information may not be widely spread in a CUT. But, the fault information may be easily propagated to a primary output.

In our testing, random patterns generated by the FPG are applied to a CUT, and then the output signals of a CUT are fed back to an LFSR. Therefore, if the fault information were propagated to a primary output, the sequence of random patterns would be changed. This means that the fault information which is propagated to a primary output is widely spread in a CUT via the FPG.

Hence, a fault near a primary input as well as a fault near a primary output can be easily detected. This fault detection mechanism is illustrated in Fig. 3.

3.3 Identification of dynamic current

The dynamic current is transformed to a voltage by a
Influence of a fault

Fig. 4 Current consumption model.

Assume 4 time units of propagation delay of a signal in each gate. It is about half of the period during which the waveform of the dynamic current exists. Here, the period during which each vector is applied is assumed to be 100 time units.

Based on these assumptions, we calculate the dynamic current of a CUT by summing up the one consumed at each gate as shown in Fig. 5. Fig. 6 shows the simulated waveform of the dynamic current of c432 when random patterns are applied. From this figure, our simulation seems to be adequate.

In our method, in advance of testing, the mean current of a fault-free CUT is measured every time when each test vector is applied. This voltage is regarded as the dynamic current in a processor for fault detection. In order to detect a fault, the dynamic current of a faulty circuit has to be distinguished from the one of a fault-free circuit. We consider the mean value represents some feature of the dynamic current. The mean current is calculated to the period during which each test vector is applied. The mean value of the dynamic current monitored in a CUT is compared with the one measured in a fault-free circuit. If the difference between the two exceeds a predetermined margin, we decide that a CUT is faulty.

4. Simulation

We performed the simulation on a 4-bit adder and some ISCAS'85 benchmark circuits[12] using the HP9000/345 workstation. We consider two cases where a gate delay is assumed and a gate delay is not assumed, because we would like to see the influence of propagation delay of signals on detectability.

4.1 In case gate delay is assumed

In this simulation, we partition the time into a number of time units, and then calculate the waveform of the dynamic current at each time unit. Fig. 4 shows the assumed current consumption model of each gate when a transition of logical value occurs at the output. The waveform continues to exist for 7 time units. We also assume 4 time units of propagation delay of a signal in each gate. It is about half of the period during which the waveform of the dynamic current exists. Here, the period during which each vector is applied is assumed to be 100 time units.

Based on these assumptions, we calculate the dynamic current of a CUT by summing up the one consumed at each gate as shown in Fig. 5. Fig. 6 shows the simulated waveform of the dynamic current of c432 when random patterns are applied. From this figure, our simulation seems to be adequate.

In our method, in advance of testing, the mean current of a fault-free CUT is measured every time when each test vector is applied. This mean current is called reference mean current. When a testing is performed, the mean current of a CUT is compared with the reference mean current. If the difference between the two exceeds predetermined margin, we decide that the CUT is faulty.
4.2 In case gate delay is not assumed

In this simulation, we evaluate the mean value of the dynamic current by counting the total number of transitions of the logical value at the output of each gate for the period during which each test vector is applied. We consider that the mean dynamic current must be proportional to the total number of transitions. This makes it possible for the simulation to be performed very fast. If the difference between the number of the transitions of a CUT and the one of a fault-free circuit exceeds pre-determined margin, we decide that the CUT is faulty.

5. Simulation results

5.1 Stuck-at fault

(a) In case gate delay is assumed

The simulation results are shown in Table 1. The margin is assumed to be 10% of the mean current which is calculated when whole test vectors are applied to a CUT. The number of applied test vectors is restricted by the simulation time, and is about twice as much as the one of the test vectors generated using the FAN algorithm[11]. The fault coverage over 95% is obtained for the circuits of a small size. For the circuits of a larger size, the fault coverage of over 90% is obtained.

Table 1 also shows the number of random patterns which a traditional random testing requires to obtain the same fault coverage. In all cases, our current testing requires less number of random patterns than the one required by a traditional random testing.

(b) In case gate delay is not assumed

The simulation results are shown in Table 2. The margin is assumed to be 5% and 10% of the mean current (actually the mean number of transitions) which is calculated when whole test vectors are applied to a fault-free circuit. We can find out that the fault coverage is lower than the one in case gate delay is assumed. Hence, the propagation delay of signals works well for detectability. However, since the obvious difference cannot be identified for c1355, we consider that the influence of gate delay on detectability is smaller as the size of a circuit becomes larger.

In case gate delay is not assumed, simulation time is much shorter than one in case gate delay is assumed. We performed the simulation such that more test vectors are applied. These results are also shown in Table 2. We can find out that the fault coverage of over 95% is obtained in all circuits.

<table>
<thead>
<tr>
<th>CIRCUIT</th>
<th>NO OF VECTORS</th>
<th>MARGIN</th>
<th>NO OF VECTORS</th>
<th>MARGIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>adder</td>
<td>20</td>
<td>94.5</td>
<td>30</td>
<td>100</td>
</tr>
<tr>
<td>c17</td>
<td>12</td>
<td>92.5</td>
<td>20</td>
<td>100</td>
</tr>
<tr>
<td>c432</td>
<td>100</td>
<td>89.5</td>
<td>1000</td>
<td>98.5</td>
</tr>
<tr>
<td>c499</td>
<td>140</td>
<td>91.5</td>
<td>1000</td>
<td>99.5</td>
</tr>
<tr>
<td>c900</td>
<td>140</td>
<td>91.5</td>
<td>1000</td>
<td>99.5</td>
</tr>
<tr>
<td>c1355</td>
<td>200</td>
<td>95.5</td>
<td>1000</td>
<td>99.5</td>
</tr>
</tbody>
</table>

We also analyzed the fault coverage when the value of the margin was increased. This means that we analyzed the fault coverage under a severer detection condition. Fig. 7 shows the relationship between the number of test vectors and the fault coverage for c432 in case the feedback from the outputs of a CUT to an LFSR exists. Fig. 8 shows the same relationship in case this feedback does not exist. The larger the margin becomes, the lower the fault coverage becomes in both cases. However, we can find out that the feedback would work well even if the detection condition were made severe, and a higher fault coverage could still be obtained owing to this feedback.

5.2 Stuck-open fault

Considering a stuck-open fault, we modified the structure of a CUT, such that an AND gate, a NAND gate and an EXOR gate are constructed using an NAND gate and a NOT gate, an NOR gate and a NOT gate, and four NAND gates, respectively. The specifics of modified circuits are shown in Table 3, where mc** denotes a modified version of c**. We consider that a fault occurs at a transistor which constitutes a gate. Gate delay is not assumed, because we would like to perform the simulation faster and to see the rough tendency of detectability. The simulation results are shown in Table 4. The margin is assumed to be 5% and 10% of the mean current which is calculated when whole test vectors are applied to a fault-free circuit.
Fig. 7 Number of test vectors vs. fault coverage for c432 in case feedback from a CUT to LFSR exists (stuck-at fault).

Fig. 8 Number of test vectors vs. fault coverage for c432 in case feedback from a CUT to LFSR does not exist (stuck-at fault).

Table 3 Specifics of modified circuits.

<table>
<thead>
<tr>
<th>CIRCUIT NAME</th>
<th>NO OF GATES</th>
<th>NO OF INPUTS</th>
<th>NO OF OUTPUTS</th>
<th>NO OF FAULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>madder</td>
<td>76</td>
<td>8</td>
<td>5</td>
<td>214</td>
</tr>
<tr>
<td>mc17</td>
<td>6</td>
<td>5</td>
<td>2</td>
<td>24</td>
</tr>
<tr>
<td>mc432</td>
<td>268</td>
<td>36</td>
<td>7</td>
<td>1092</td>
</tr>
<tr>
<td>mc499</td>
<td>572</td>
<td>41</td>
<td>32</td>
<td>2140</td>
</tr>
<tr>
<td>mc880</td>
<td>555</td>
<td>60</td>
<td>26</td>
<td>1802</td>
</tr>
<tr>
<td>mc1355</td>
<td>636</td>
<td>41</td>
<td>32</td>
<td>2308</td>
</tr>
</tbody>
</table>

Table 4 Simulation results for a stuck-open fault in case gate delay is not assumed.

<table>
<thead>
<tr>
<th>CIRCUIT NAME</th>
<th>NO OF VECTORS</th>
<th>5% COVERAGE</th>
<th>10% COVERAGE</th>
<th>RANDOM TESTING</th>
</tr>
</thead>
<tbody>
<tr>
<td>madder</td>
<td>50</td>
<td>94.9</td>
<td>94.9</td>
<td>94.9</td>
</tr>
<tr>
<td>mc17</td>
<td>20</td>
<td>91.7</td>
<td>89.3</td>
<td>89.3</td>
</tr>
<tr>
<td>mc432</td>
<td>1000</td>
<td>85.8</td>
<td>83.6</td>
<td>82.9</td>
</tr>
<tr>
<td>mc499</td>
<td>1000</td>
<td>89.5</td>
<td>89.3</td>
<td>81.4</td>
</tr>
<tr>
<td>mc880</td>
<td>1000</td>
<td>89.1</td>
<td>88.4</td>
<td>88.1</td>
</tr>
<tr>
<td>mc1355</td>
<td>1000</td>
<td>90.0</td>
<td>89.8</td>
<td>89.6</td>
</tr>
</tbody>
</table>

Fig. 9 Number of test vectors vs. fault coverage for c432 in case feedback from a CUT to LFSR exists (stuck-open fault).

Fig. 10 Number of test vectors vs. fault coverage for c432 in case feedback from a CUT to LFSR does not exist (stuck-open fault).

fault is assumed, it turns out that the feedback does work well, and a higher fault coverage can still be obtained owing to this feedback.

6. Discussion

In order to investigate what kind of a circuit our current testing can be effectively applied, we considered two sample circuits of NAND gates, that are named WIDE and DEEP respectively, and analyzed their fault coverage.
have about the same number of gates and lines, but their deep circuit.

and shallow circuit, and a DEEP is referred to a narrow and deep circuit. Hence, a WIDE is referred to a wide and shallow circuit. In both circuits, the fault coverage of our current testing is higher than the one of a WIDE. Therefore, our testing seems to be effectively applicable for a deep and narrow circuit.

Fig. 11 also shows the fault coverages of the two circuits in case a traditional random testing is applied. In both circuits, the fault coverage of our current testing is higher than the one of a traditional random testing. It is interesting that the relationship between the fault coverage of a DEEP and the the one of a WIDE is reverse between our current testing and in a traditional random testing.

7. Conclusion

In this paper, we proposed a current testing using random patterns and monitoring the dynamic current, where a stuck-at fault and a stuck-open fault are assumed. We found out that the feedback from the outputs of a CUT to an LFSR works well, and a high fault coverage can be obtained applying a small number of test vectors. This testing turned out to be a promising candidate of a testing for CMOS logic circuits.

In order to determine whether the dynamic current is normal or not, we discussed such a simple method as calculating the mean dynamic current. When performing the current testing in practical use, we cannot neglect the disturbances in a current measuring system, and the fluctuation of parameters in a circuit. We have to discuss how to meet with these problems. We are now making the research that a neural network is used to identify the difference between the waveform of a fault-free circuit and the one of a faulty circuit. This is because we consider that the neural network is suitable for extracting the features of the waveform more powerfully.

Also we would like to discuss the application of our current testing to a gate-oxide short fault and a bridging fault[13,14] in addition to a stuck-at fault and a stuck-open fault.

References


Table 5 Specifics of sample circuits WIDE and DEEP

<table>
<thead>
<tr>
<th>CIRCUIT NAME</th>
<th>NO. OF INPUT</th>
<th>NO. OF OUTPUTS</th>
<th>NO. OF GATES</th>
<th>NO. OF LINES</th>
</tr>
</thead>
<tbody>
<tr>
<td>WIDE</td>
<td>8</td>
<td>8</td>
<td>105</td>
<td>371</td>
</tr>
<tr>
<td>DEEP</td>
<td>8</td>
<td>8</td>
<td>105</td>
<td>385</td>
</tr>
</tbody>
</table>

The specifics of the circuits are shown in Table 5. They have about the same number of gates and lines, but their number of primary inputs and primary outputs are different to each other. Hence, a WIDE is referred to a wide and shallow circuit, and a DEEP is referred to a narrow and deep circuit.

Fig. 11 shows the simulation results for a stuck-at fault in case gate delay is assumed. The fault coverage of a DEEP is higher than the one of a WIDE. Therefore, our current testing seems to be effectively applicable for a deep and narrow circuit.

Fig. 11 also shows the fault coverages of the two circuits in case a traditional random testing is applied. In both circuits, the fault coverage of our current testing is higher than the one of a traditional random testing. It is interesting that the relationship between the fault coverage of a DEEP and the the one of a WIDE is reverse between our current testing and in a traditional random testing.

The current testing in practical use, we cannot neglect the disturbances in a current measuring system, and the fluctuation of parameters in a circuit. We have to discuss how to meet with these problems. We are now making the research that a neural network is used to identify the difference between the waveform of a fault-free circuit and the one of a faulty circuit. This is because we consider that the neural network is suitable for extracting the features of the waveform more powerfully.

Also we would like to discuss the application of our current testing to a gate-oxide short fault and a bridging fault[13,14] in addition to a stuck-at fault and a stuck-open fault.

References