INVITED TALK 2

Statistical Device Variability and its Impact on Design

Asen Asenov
Device Modelling Group
Department of Electronics and Electrical Engineering,
University of Glasgow, Glasgow, G12 8LT
Tel: 0141 330 4790, E-mail: A.Asenov@elec.gla.ac.uk

Abstract

It is widely recognized that the uncontrollable statistical variability in device characteristics represent major challenges to scaling and integration for present and next generation nano-CMOS transistors and circuits. This will in turn demands revolutionary changes in the way in which future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and fundamental device technology to allow circuits and systems to accommodate the increasing statistical variability. This will add significant complexity to the design process, requiring orchestration of a broad spectrum of design tools by geographically distributed teams of device experts, circuit and system designers.

In this talk we review the major sources of variability in CMOS devices focusing at and beyond 45nm technology generation and beyond. The focus is on intrinsic parameter fluctuations introduced by discreteness of charge and matter, which play an increasingly important role in the present and future CMOS devices and cannot be controlled or reduced by tightening the process tolerances. One of the most important sources of intrinsic parameter fluctuations illustrated in are the random discrete dopants in combination with line edge roughness (Fig. 1) and the poly silicon gate granularity (Fig. 2) which makes every transistor microscopically different from its counterparts and introduces differences in the characteristics of topologically identical devices (Fig. 3). The corresponding parameter variations already affect adversely the yield and the functionality and limit the scalability of SRAM cells. We will present results forecasting the magnitude of the statistical device variability in the next technology generations based on comprehensive physical 3D statistical simulation. A methodology for transferring of this information into industry standard compact models like BOSIM4 and BISIMSOI will also be presented. The use of compact models in statistical circuit simulations will be illustrated in the case of SRAM design.
Biography

Asen Asenov received his MSc degree in solid state physics from Sofia University, Bulgaria in 1979 and the PhD degree in physics from The Bulgarian Academy of Science in 1989. He is a professor of Device Modelling, Leader of the Glasgow Device Modelling Group and Academic Director of the Glasgow Process and Device Simulation Centre he coordinates the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. He has pioneered the simulations of statistical variability in nano-CMOS devices including random dopants, interface roughness and line edge roughness. He has over 400 publications in the above areas.