Testing Asynchronous Circuits: Help is on the Way!

Ajay Khoche

DFT Scientist

Agilent Laboratories

Abstract

Testing of asynchronous circuits is considered to be a difficult task. The presence of asynchronous components in an Integrated Circuit (IC), let alone the whole IC itself, sends shivers into any test manager. This general sense of difficulty can be attributed to lack of understanding, lack of interest, lack of support from various players in the testing game including Automated Test Equipment (ATE) vendors.

However designs are more and more starting to have asynchronous looks. The device size, the performance specs are making the signals appear as asynchronous. In addition the design styles like SoC (System on a Chip) and SoP (System on a Package) may attract the asynchronous communications among the blocks, which constitute these systems. Also going forward, International Technology Roadmap for Semiconductors predicts the need for systems that do not require system wide synchronicity. It also asks for block level handshaking protocols.

Test Community is responding to the design changes by supporting various features either on-chip or on ATEs to enable testing of these devices. Therefore even though the test community is not directly addressing the problems of testing asynchronous circuits one can expect support for various features that will help in the testing of asynchronous circuits in general.

In this talk I will describe the synergies in test problems with synchronous designs that will help in testing of asynchronous designs. In particular, I will touch upon the ATE architectures and point out where the current architectures are inadequate in supporting testing of asynchronous circuits. I will then describe the current and planned features in ATEs that will be helpful in testing asynchronous circuits.

I will then describe test/manufacturing flow for a typical IC and point out the gaps that will have to be bridged to make testing of asynchronous circuits practical. In this portion of the talk, I will cover various topics including Design for Testability, Test Generation, Test translation, Test time management, where the development in synchronous circuit domain can be used as platform to build similar capabilities for asynchronous circuits.