Asynchronous Design and the Pursuit of Low Power

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Two often cited arguments for the inherent low-power benefit of asynchronous or self-timed design is that the clock signals cause unnecessary switching activity and that the clock signals themselves dissipate a large portion of the total chip power. However, the careful and explicit application of conditional clocking and the use of novel clock driver circuits in synchronous designs rival the asynchronous approaches without incurring the typical circuitry overhead of asynchronous design. There are still though some avenues to pursue in exploiting the low-power advantages of asynchronous and self-timed circuit concepts. One promising avenue is the use of self-timed postcharged logic, sometimes called "self-resetting" logic, which has proven to be highly effective in RAM design and could possibly extend to other kinds of computing structures.