Keynote Speaker Abstracts

Keynote Session I
The 2000 MHz Bug- End of the Millennium of Synchronous Systems?
   Richard F. Lyon

Abstract. This year puts us in mind of problems involving the approach of the number 2000, so I thought it would be good to examine the relevance of this number to asynchronous logic. I could have picked a 2000-ps clock period, but since we approach that from above, and since we’re basically there already with modern synchronous processors, I thought I better take a look at 2000 MHz. It would be rash to claim that asynchronous techniques might get us there more easily than synchronous, but maybe it would be more realistic to say that synchronous systems at such speeds are just going to be nearly impossible to design, build, and keep working. So maybe there will be a time when logic is so fast, and systems are so slow by comparison, that the asynchronous style will no longer have a speed penalty and the advantages of configurability, stability, low power, etc., will shine through. But that time will only come if we find a way to propagate a design style through the schools and companies that make chips, subsystems, etc. In my recent experience, I find young designers who are very good with synchronous systems, yet who have never heard of our friends Charlie Molnar and synchronizer failure, both of whom are eternal. They build systems with too many crystal oscillators-and somehow make them work (most of the time). Designs such as synchronous pipelined A/D converters that can’t work in theory are doing pretty well in practice, with only a few values being corrupted by metastability. There may be an opportunity here if we can educate people just as the problems become severe enough to get their attention. I said about the same thing at the 1993 ASYNC meeting, and I’m eager to get caught up on the progress in implementations and education at this millenium-concluding meeting.

Keynote Session II
Exploiting BDDs in Higher Order Logic, with Applications to Asynchronous Circuits
   Mike Gordon

Abstract. A theorem prover enhanced with BDD-based symbolic state enumeration will be described. An asynchronous arbiter circuit, previously analysed algorithmically (by Lee, Greenstreet, and Seger), will be used as an example.

Keynote Session III
Asynchronous Macromodules Were a Pain to Build But a Joy to Use
   Wesley A. Clark

Abstract. This talk by Prof. Clark is expected to be about the early history of asynchronous macromodules—an era in which he and the Late Prof. Charles Molnar pioneered many of the foundational ideas of our field. Unfortunately, an abstract from the author was not available in time for publication.