Message from the Chairs

Welcome to the Second International Symposium on Advanced Research in Asynchronous Circuits and Systems, and welcome to Aizu-Wakamatsu! We hope that you enjoyed the view of the beautiful mountains around, and that you will enjoy it even more closely during the social events at the end of this busy week. The samurai spirit that still lingers around this city is very appropriate to our fight against the omnipresent and, apparently, omnipotent clock demon.

This is the latest, but hopefully not the last, of a series of symposia, workshops and working conferences devoted to asynchronous hardware design. The series began in 1993, with the Manchester Working Conference, continued in 1994 with the Utah Symposium, and in 1995 with the Nof Ginosar Workshop and the London Working Conference.

Interest in the academic community for asynchronous research is very strong, as indicated by the growing number of publications in recent years (1 book and 34 papers in 1991, 1 book and 41 papers in 1992, 1 book and 71 papers in 1993, 2 books and 92 papers in 1994, 2 books and 74 papers in 1995, according to a major bibliographical database). The field is characterized by a strong theoretical background (stronger, in some sense, than in synchronous design) accompanied by very practical orientations.

Theory and practice notwithstanding, industrial interest for asynchronous design techniques seems so far to be limited to few pilot projects. The usual motivations of modularity, power consumption, speed, and so on do not seem to be critical enough to push towards a major methodology change. This lack of industrial relevance is problematic for at least two reasons. First, it obviously causes funding problems. Second, it drastically reduces the number of significant, interesting examples to which methods and tools can be applied. In our opinion, the asynchronous community has several (mutually compatible) options to tackle the problem:

- To keep developing solid work and wait for the problems associated with clock distribution to really become unmanageable. This approach has some appeal, and may become successful even in the short term when deep sub-micron processing facilities will become operational. It may be significant especially for low-production designs that cannot afford to pay very high non-recurrent engineering costs.

- To look at more exotic device implementation techniques that may become practical in the medium and long term. Quantum devices, for example, may be a fruitful source of problems that require a truly clock-less solution.

- To cross-fertilize with other areas in which the synchronous hypothesis is definitely too expensive to implement. In particular, it is interesting to observe that some of the most successful specification techniques for asynchronous circuits are based on Hoare’s Communicating Sequential Processes that were originally born for programming reliable distributed software systems.

The committee organizing this symposium tried to put together a program that, while rich in new and promising ideas, could also appeal to more practically oriented designers. The first day will be devoted to tutorials, exploring new potential areas of application, as well as surveying methods by which designers can solve some of today’s problems that are not tackled by
commercial design systems. The second, third and fourth day will be devoted to technical sessions, invited talks and social events. There will also be opportunities to demonstrate CAD tools, in order to dispel the myth that asynchronous design is some sort of black magic art, for which no automated aid exists.

A total of 60 papers were submitted to the symposium (a good number, considering that two other workshops on asynchronous circuits were held this year). Each paper was anonymously reviewed by 4 or 5 members of the technical committee, and the final list was decided after several exchanges of electronic mail messages among the committee members. We accepted 24 papers for publication in the proceedings. There will also be an opportunity to present less mature research in poster sessions.

We would like to thank first of all the Technical Committee members for their dedication that has made the severe and timely selection process possible. Then we would like to thank the IEICE Technical Group on VLSI Design, the Telecommunications Advancement Foundation, the IFIP WG 10.5, and the University of Aizu (in particular Yuko Kesen and Kazuaki Yamauchi) for their financial and organizational support. Many thanks go to the IEEE Computer Society (in particular to Penny Storms) for their help in preparing the proceedings. Last but not least, we thank and congratulate the researchers who made this symposium possible by their daily work, by thinking, implementing and... writing.